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Inverted-Type InGaAs Metal–Oxide–Semiconductor High-Electron-Mobility Transistor on Si Substrate with Maximum Drain Current Exceeding 2 A/mm

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Inverted-type $In_{0.51}Al_{0.49}As/In_{0.53}Ga_{0.47}As$ metal–oxide–semiconductor high-electron-mobility transistor grown by metal organic chemical vapor deposition on a Si substrate was demonstrated. 8 nm atomic-layer-deposited Al_2O_3 was used as gate dielectric. N^{++} InGaAs with an electron density of 4.5×10^{19} cm^{-3} was selectively regrown in the source/drain regions to reduce parasitic resistance while eliminating the conventional gate recess etching. 130-nm channel-length devices have exhibited a drain current up to 2.03 A/mm at $V_{ds} = 0.6$ V and an ultralow on-resistance of 163 Ω μm. An effective mobility of 2975 cm^2 V^{-1} s^{-1} was also extracted, indicating the high-quality epitaxial growth by metal organic chemical vapor deposition. © 2012 The Japan Society of Applied Physics

Si complementary metal oxide semiconductor (CMOS) scaling is now in a new phase of "power constrained scaling" in which the power dissipation has hit a limit of 100 W/cm^2.[1] In order to reduce power consumption while maintaining high-speed operation, high on-current at low supply voltage is required for future transistors. According to the International Technology Roadmap for Semiconductors (ITRS) 2010,[2] the saturation drain current should exceed 2 A/mm at $V_{ds} = 0.6$ V. Recently there has been much interest generated in the research of non-silicon electronic materials and novel devices for future high-speed and ultralow-power logic applications. High-mobility III–V field-effect transistors (FET) is a promising candidate and significant progress has been achieved. However, most of these devices were grown by molecular beam epitaxy (MBE) on InP substrates. InP substrate is not suitable for future VLSI application due to its high cost, small size and brittleness. Meanwhile, Si remains the workhorse in the IC industry and will continue to progress in its manufacturing technologies in the foreseeable future. To combine the superior carrier transport properties of III–V compounds with Si technologies, one straightforward wafer-level solution is III–V heteroepitaxy on Si substrate.[3–6] Compared with MBE, metal organic chemical vapor deposition (MOCVD) is preferred for high-volume manufacturing. In this work, 130-nm channel-length InGaAs metal–oxide–semiconductor high-electron-mobility transistor (MOSHEMT) on Si substrate grown by MOCVD with significantly boosted on-state performance was demonstrated.

It was reported in previous studies that source/drain (S/D) doping concentrations up to 10^{20} cm^{-3} are required for high injection current without source starvation.[7,8] However, the peak donor concentration in InGaAs S/D formed by conventional ion implantation was around 1×10^{19} cm^{-3} due to the limited activation efficiency,[9] which made the access resistance of inversion-mode metal–oxide–semiconductor field-effect transistor (MOSFET) relatively large. InAlAs/InGaAs quantum-well FET is another attractive candidate because of its superior effective electron mobility and flexibility in band structure engineering. However, the conventional HEMT or MOSHEMT featuring a recessed gate may be difficult for VLSI application due to the large footprint and etching depth variation. One emerging alternative device design is to incorporate regrown S/D for ohmic contacts, thereby eliminating gate recess etching. In this work, selective source/drain regrowth by MOCVD was employed in the InAlAs/InGaAs MOSHEMT fabrication.

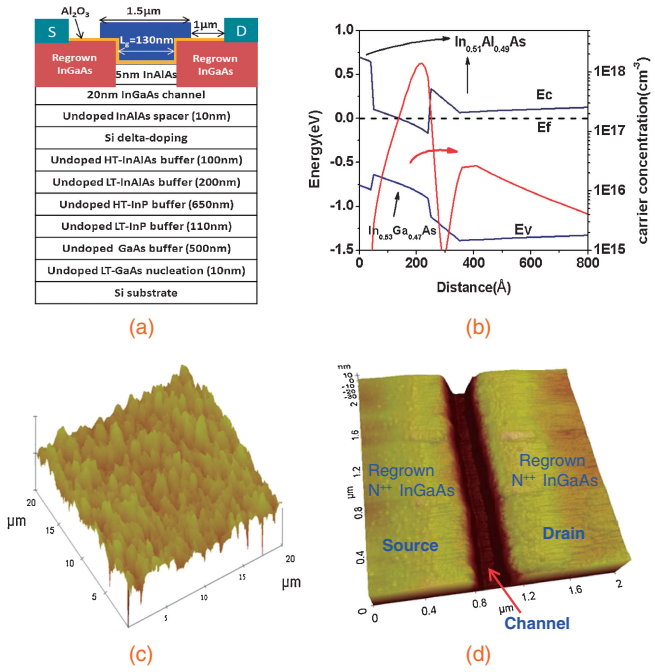

Fig. 1. (a) Schematic cross section of a finished device (LT: low temperature, HT: high temperature, note: figure is not drawn to scale). (b) Simulation of the band structure and carrier distribution of the InAlAs/InGaAs heterostructure. (c) AFM image of the HEMT epitaxial layer across a scanned area of 20 × 20 μm^2. (d) AFM image of the regrown S/D separation after the gate oxide deposition.

A 4-in. exact-(001)-oriented Si substrate was used in our experiment. The Si wafer was cleaned using an $NH_4OH : H_2O_2 : H_2O$ (1 : 1 : 5) boiling solution first, followed by a $HF : H_2O$ (1 : 40) dip. Epitaxial growth was carried out in an Aixtron 200/4 MOCVD system. Si wafer was annealed at 810 °C in H_2 for 30 min, and AsH_3 was introduced at the end of the annealing. The composite buffer stack consists of 10 nm GaAs nucleation layer deposited at 400 °C, 500 nm GaAs grown at graded temperatures of 550, 590, and 630 °C, 110 nm InP nucleation layer deposited at 450 °C, 650 nm InP grown at 600 °C and 300 nm $In_{0.51}Al_{0.49}As$ buffer layer. The inverted-type InAlAs/InGaAs HEMT structure includes a 5 nm $In_{0.51}Al_{0.49}As$ cap layer, a 20 nm $In_{0.53}Ga_{0.47}As$ channel and a 10 nm $In_{0.51}Al_{0.49}As$ backside spacer. Si delta-doping was inserted under the $In_{0.51}Al_{0.49}As$ spacer. Figure 1(a) shows the cross-sectional schematic of the layered structure, and Fig. 1(b) gives a

simulation of the corresponding band structure and carrier distribution. Figure 1(c) shows the atomic force microscopy (AFM) image of the entire device stack across a scanned area of $20 \times 20\,\mu m^2$, and the RMS value of 4.8 nm was measured, similar to MBE growth results.[6] From room-temperature Van der Pauw Hall measurements, an electron mobility of $4100\,cm^2\,V^{-1}\,s^{-1}$ with sheet carrier concentration of $4.02 \times 10^{12}/cm^2$ was obtained, which combined into a sheet resistance of $379\,\Omega/sq$.

A gate-last non-self-aligned process was developed to fabricate MOSHEMTs with regrown S/D. The as-grown HEMT wafer was first passivated by SiO_2 (1000 Å) as re-growth mask. Then the SiO_2 was patterned by buffered oxide etch (BOE), followed by S/D recess etching down to the InGaAs channel using a $H_3PO_4 : H_2O_2 : H_2O$ (3 : 1 : 50) solution. All the 5 nm InAlAs and around 10 nm of the InGaAs channel were removed. The recess etch is not critical as long as it terminates somewhere within the channel. Then 60 nm of Si-doped InGaAs with an electron concentration of 4.5×10^{19} cm^{-3} was regrown in the exposed S/D regions by MOCVD at 600 °C, using TEGa, TMIn, TBA, and SiH_4 as precursors. The growth rate was around 15 nm/min and (111) sidewall growth facets were observed. The SiO_2 growth mask was removed by BOE and mesa isolation was formed by wet etching down to the InAlAs buffer. The gate width was defined by the mesa width, which was designed to be 10 µm but shrunk to 9.57 µm due to the lateral etch undercut. After surface cleaning using $HCl : H_2O$ (1 : 10) for 2 min followed by $(NH_4)_2S$ passivation for 15 min, the sample was immediately loaded into an Oxford OpAL atomic layer deposition (ALD) system. *In-situ* trimethylaluminum (TMA) pretreatment was performed in the ALD chamber using ten cycles of TMA/Ar, i.e., 30 ms TMA pulse followed by 3 s Ar purge for one cycle. This *in-situ* TMA pretreatment was believed to be an effective passivation method to improve the gate dielectric/III–Vs interface.[10–13] Then 8 nm of Al_2O_3 was deposited on the sample at 300 °C using TMA and water as precursors, followed by post deposition annealing (PDA) at 380 °C for 30 min using H_2 in the ALD chamber. Source/drain contact holes were subsequently opened, and non-alloyed ohmic contacts were achieved by electron beam evaporation of Ni/Ge/Au/Ge/Ni/Au and lift off process. Finally, Ti/Pt/Au gate metallization was realized. The cross-sectional view of the device after fabrication process is depicted in Fig. 1(a). The fabricated device had a channel length of 130 nm, which was defined by the AFM measurement of the regrown source/drain separation after the gate oxide deposition, as illustrated in Fig. 1(d).

The output and transfer characteristics of a 130-nm channel-length device are shown in Fig. 2. The maximum drain current ($I_{ds,max}$) of 2.03 A/mm was obtained at $V_{gs} =$ 2 V and $V_{ds} = 0.6$ V, and the peak extrinsic transconductance ($G_{m,max}$) of 744 mS/mm was achieved at $V_{ds} = 0.5$ V. The threshold voltage is determined to be −2.9 V, using linear extrapolation from I_{ds}–V_{gs} curve at $V_{ds} = 50$ mV. The gate leakage current was 6.17×10^{-7} A/mm at $V_{gs} = 2$ V and $V_{ds} = 0.6$ V, which was over six orders smaller than the $I_{ds,max}$ of 2.03 A/mm obtained at the same bias. An ultralow R_{on} of 163 Ω µm was extracted from the I_{ds}–V_{ds} curve, which could be attributed to the raised S/D with high doping level.

To evaluate the quality of selective S/D regrowth, two transmission line matrix (TLM) patterns were designed

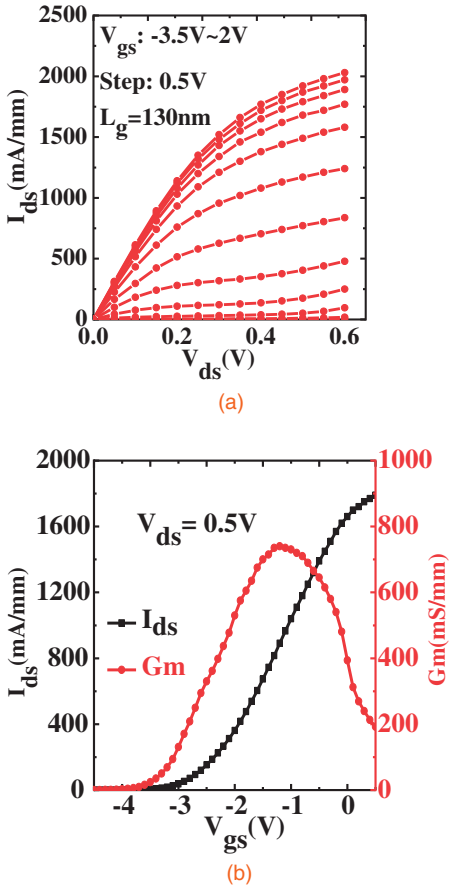

Fig. 2. (a) Output characteristic of a device with $L_g = 130$ nm. (b) Transfer characteristics of a device with $L_g = 130$ nm at $V_{ds} = 0.5$ V.

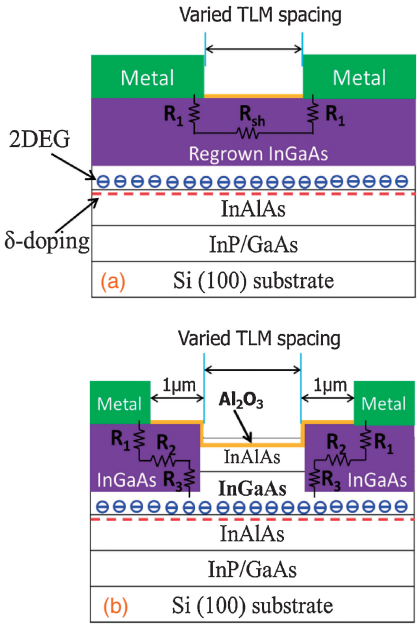

Fig. 3. Extraction of access resistance using TLM-1 (a) and TLM-2 (b).

as illustrated in Fig. 3. The access resistance components, including the contact resistance (R_1) between the S/D metal and regrown InGaAs, series resistance (R_2) of the regrown InGaAs, and the regrowth interface resistance (R_3) caused by interfacial defects could be extracted by TLM measure-

Table I. Comparison of R_{on} and on-current at a drain bias of 0.5 V for InGaAs channel FETs (D: depletion, E: enhancement, R: reference).

Ref.	L_g (nm)	Substrate	Mode	Oxide	I_{ds} ($V_{ds} = 0.5$ V) (mA/mm)	R_{on} ($\Omega\,\mu$m)
14	160	InP	E	Al_2O_3	467	1071
15	1000	InP	E	Y_2O_3/Al_2O_3	555	938
16	200	InP	E	Al_2O_3	437	737
17	100	InP	D	Al_2O_3	944	496
18	50	InP	D	Al_2O_3	2400	160
19	55	InP	E	Al_2O_3/HfO_2	1756	199
20	60	InP	D	Al_2O_3	978	341
This work	130	Si	D	Al_2O_3	1920	163

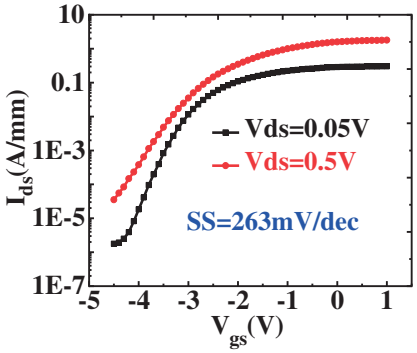

Fig. 4. Subthreshold characteristics of a device with $L_g = 130$ nm at $V_{ds} = 0.5$ V and $V_{ds} = 0.05$ V.

ment. The average sheet resistance of the regrown $In_{0.53}Ga_{0.47}As$ ($R_{sh} = 21.8\,\Omega/\square$) and $R_1 = 8.5\,\Omega\,\mu$m were determined from TLM-1, while average values of $R_2 = 21.8\,\Omega\,\mu$m and $R_3 = 30.5\,\Omega\,\mu$m were deduced from TLM-2. The total access resistance of $2(R_1 + R_2 + R_3)$ ranged from 114 to 132.3 $\Omega\,\mu$m across the sample with an average value of 121.5 $\Omega\,\mu$m, which agreed well with the R_{on} of 163 $\Omega\,\mu$m.

Table I gives a comparison of R_{on} and $I_{ds,max}$ at a low supply voltage of $V_{ds} = 0.5$ V for the recently reported InGaAs MOSFETs.[14–20] Although the devices reported in this work were metamorphically grown on Si substrates, which inevitably have more dislocations in the active layers and rougher surface than lattice-matched ones on InP substrates, they still exhibit attractive current drivability and low R_{on}. This reflects the high-quality growth of metamorphic devices lattice-matched to InP on Si substrates and selective InGaAs regrowth by MOCVD.

Figure 4 shows the subthreshold characteristics of a 130-nm channel-length device. The subthreshold slope (SS) was 263 mV/dec at $V_{ds} = 50$ mV. Another device with longer channel length of 1 μm exhibited a similar SS of 254 mV/dec at $V_{ds} = 50$ mV. The current SS and large gate bias swing are believed to be limited by the capacitance equivalent thickness (CET) arising from the thick Al_2O_3 gate dielectric and InGaAs channel. More efforts are required to improve the gate electrostatic control over channel. Effective mobility (μ_{eff}) was extracted as a function of carrier density using a combination of 1 MHz capacitance–voltage (C–V)

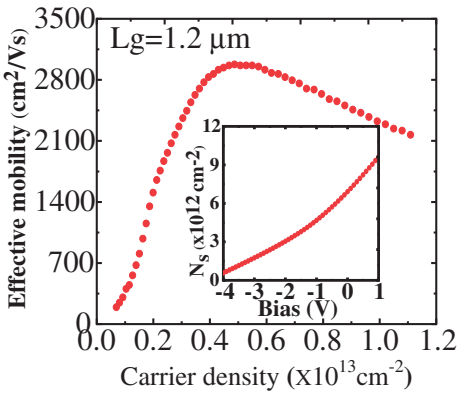

Fig. 5. Effective mobility as a function of carrier density. Inset: carrier density profile.

and I_{ds}–V_{ds} measurement.[21] Although the μ_{eff} extracted from short-channel devices is usually underestimated when compared to that extracted from long-channel devices, a peak μ_{eff} of 2975 $cm^2\,V^{-1}\,s^{-1}$ was still obtained for a 1.2 μm gate-length InGaAs MOSHEMT as shown in Fig. 5, indicating the high-quality epitaxial growth by MOCVD.

In summary, InAlAs/InGaAs MOSHEMTs on Si substrates grown by MOCVD have been demonstrated. Selective regrowth was incorporated to minimize the access resistance while eliminating gate recess etching. An $I_{ds,max}$ of 2.03 A/mm was achieved at $V_{ds} = 0.6$ V. Ultralow on-resistance and contact resistance were obtained. Our results indicate that combining the InAlAs/InGaAs HEMT structure with source/drain regrowth is promising for high drive current operation at low supply voltage.

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