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Effect of post-gate RTA on leakage current (I_{off}) in GaN MOSHEMTs

Tongde Huang, Ka Ming Wong, Ming Li, Xueliang Zhu, and Kei May Lau*

Department of Electronic and Computer Engineering, Hong Kong University of Science & Technology, Clear Water Bay, Hong Kong

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* Corresponding author: e-mail eekmlau@ust.hk, Phone: +852-2358-7049, Fax: +852-2358-1485

Effect of post-gate rapid thermal annealing (RTA) on GaN metal-oxide semiconductor high electron mobility transistors (MOSHEMTs) performance has been investigated. For devices with 1-μm gate length and 10-μm gate width, a significant reduction of I_{off} from 10^{-4} to 10^{-6} mA/mm (at V_{gs} = -8 V, V_d = 6 V) was observed after post-gate RTA at 600 °C, indicating an excellent ON/OFF drain current ratio (I_{on}/I_{off}) up to 10^8. The reduction of I_{off} is mainly dominated by the decreased reverse-biased gate leakage current, as indicated by the strong dependence of I_{on}/I_{off} on reverse-biased gate leakage current. The reduced gate leakage after post-gate RTA probably stems from the increased gate barrier height as a result of gate metal reaction with Al_2O_3. The degradation in pulse *I-V* characteristics may be due to defect formation in devices during post-gate RTA at 600 °C. Nearly complete recovery was achieved by further post-gate RTA at 400 °C for 10 minutes.

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1 Introduction

GaN HEMTs have demonstrated outstanding performance for high frequency and high power applications, including an output power density more than 10 W/mm at 40 GHz [1], in excess of 2 W/mm at 80.5 GHz [2], and a reported power-gain cutoff frequency of 300 GHz [3]. In spite of great progress over the last two decades, several challenges still need to be overcome to improve transistor performance even further. Apart from the understanding of failure mechanism in GaN power transistors, the other major challenge is the reduction of I_{off}. A large I_{off} would not only degrade transistor reliability, but also increase standby power loss. In order to reduce I_{off} and enable a better performance, a couple of approaches have been employed in GaN HEMTs, including oxygen plasma treatment [4, 5] and post-gate RTA [6]. Another convenient way to reduce I_{off} is by insertion of a gate dielectric to block the schottky gate tunneling current, as in MOSHEMTs structure. Several groups have reported the effectiveness of gate oxide to suppress I_{off} in GaN MOSHEMTs [7, 8].

In this paper, the I_{off} in GaN MOSHEMTs was further reduced by more than one order of magnitude after post-gate RTA. The effects of post-gate RTA on other device properties were also explored, such as pulse *I-V* characteristics.

2 Experimental

The $Al_{0.3}Ga_{0.7}N$/GaN epitaxial wafer in this study was grown by metal-organic chemical vapor deposition (MOCVD) on a 2-inch (111) silicon substrate. The epitaxial layer structure consists of a 40-nm AlN nucleation layer, an 800-nm undoped GaN layer, a AlN (20 nm)/AlGaN (250 nm) interlayer, a 125-nm Mg-doped buffer layer, 875-nm undoped GaN layer, an AlN spacer layer around 1 nm, and finally a 20-nm AlGaN barrier layer. The Mg-oped GaN buffer was introduced to enhance the buffer resistivity by compensating the unintentional donors. The fabrication of MOSHEMTs began with mesa etching for device isolation (mesa depth ~120 nm) using Cl_2/He plasma in an inductively coupled plasma reactive ion etching (ICP-RIE) system. Then, Ti/Al/Ni/Au (20/150/500/-800 nm) was deposited by e-beam evaporation and annealed in RTA in a nitrogen atmosphere to form source and drain ohmic contacts. The typical ohmic contact resistance was measured to be ~0.7 Ω·mm. To avoid contamination of source/drain metal to the atomic-layer-deposition (ALD) chamber, the sample was covered by a protective layer of SiO_2 prior to Al_2O_3 gate dielectric layer deposition. SiO_2 over the gate region was then removed by buffered oxide etchant (BOE) solution. After that, 10-nm of Al_2O_3 was deposited by plasma enhanced ALD

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(PEALD). The Schottky gate contact was formed by e-beam evaporation of Ni/Au and lift-off. Moreover, in order to investigate effects of thermal treatment on the I_{off} in GaN MOSHEMTs, the wafer was cleaved into several pieces for post-gate RTA and post-deposition annealing (PDA) in a nitrogen atmosphere. For PDA at 400 to 600 °C before gate deposition, no obvious reduction of I_{off} was observed, and it was the same result for post-gate RTA for temperatures below 600 °C. In contrast, it was found that only post-gate RTA at 600 °C for 10 to 30 seconds could reduce the I_{off} effectively.

3 Results and discussion

As shown in Fig. 1, the I_{off} in GaN MOSHEMTs was reduced by almost two orders of magnitude after post-gate RTA at 600 °C for 10 seconds. The gate leakage current is also plotted to show that the I_{off} is dominated by the reverse-biased gate leakage current. The forward-biased gate leakage current increases a little bit after the post-gate RTA, which is mainly caused by the gate sink effect as a result of Ni reaction with Al_2O_3.

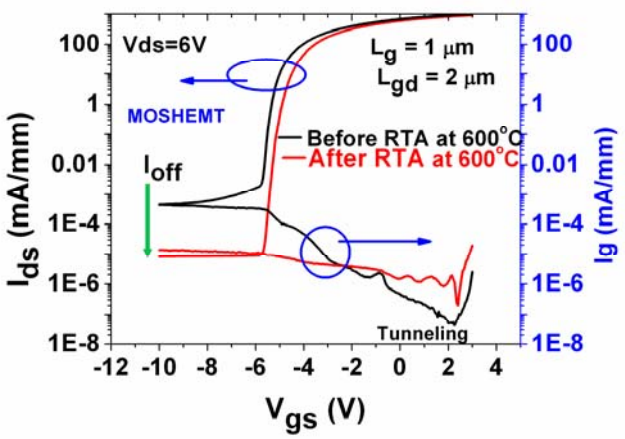

Figure 1 Transfer characteristics (semi-log-scale) and gate current of sample before and after post-gate RTA at 600 °C.

The gate sink effect induces a decrease of the gate-channel distance, which also could be confirmed by the positive shift of threshold voltage (V_{th}). The shift is around 0.5 V (Fig. 2). However, the access resistance (includes source and drain resistance) increased by about 9% after the post-gate RTA (Fig. 3). The access resistance is extrapolated from the on-state resistance curves as a function of gate overdrive voltage. As a result, extrinsic peak transconductance (G_m) shows no obvious increase even after gate sink, as compared in Fig. 2.

Figure 4 shows a common tendency that the I_{off} is reduced by more than one order of magnitude after post-gate RTA, while the I_{on} does not decrease much. The I_{off} and I_{on} were measured at V_{gs}- V_{th} = -3 V, and V_{gs}- V_{th} = 7 V respectively, at a constant drain bias of V_{ds} = 6 V.

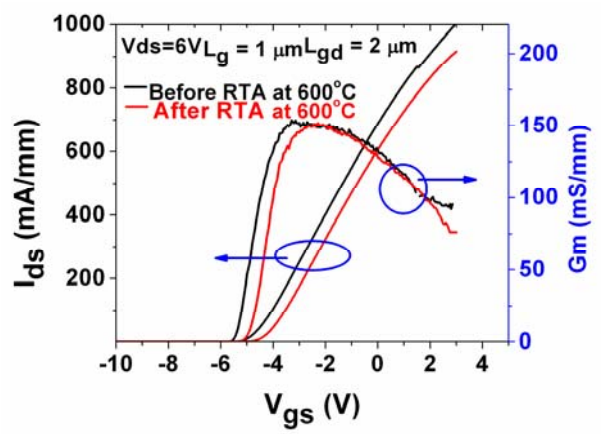

Figure 2 Transfer characteristics (linear-scale) of samples before and after post-gate RTA.

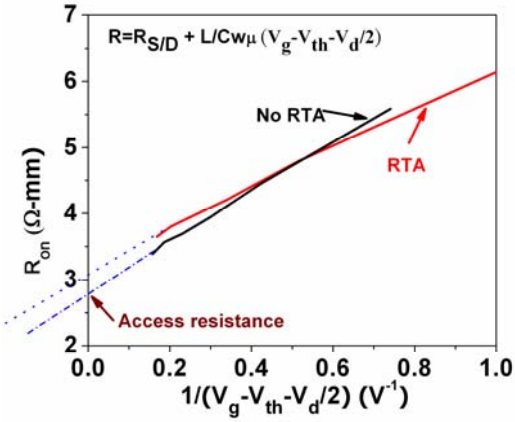

Figure 3 Slight increase in access resistance extrapolated from on-state resistance of samples before and after post-gate RTA.

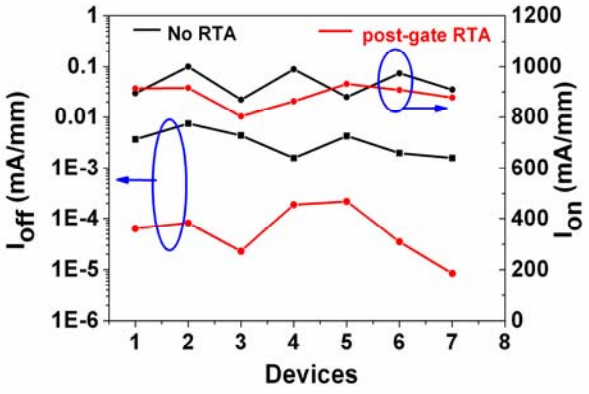

Figure 4 I_{on} and I_{off} distribution in devices across the samples before and after post-gate RTA.

As highlighted in Fig. 5, there is a strong correlation between I_{on}/I_{off} and gate leakage current. These results demonstrate that the post-gate RTA is a very effective way to lower gate leakage current (< 10^{-5} mA/mm) and increase I_{on}/I_{off} (10^7-10^8). Related to the decreased I_{off} after post-gate RTA, the breakdown voltage of the devices also increased by 30% to 130 V in this study.

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The gate leakage current (I_g) in samples under different thermal treatments was compared (Fig. 6). Compared with HEMTs made with the same structure, GaN MOSHEMTs shows obvious lower leakage current after insertion of a layer of gate oxide. The GaN HEMTs were fabricated with the same process but without gate oxide. Moreover, in contrast to samples before RTA and with PDA at 600 °C, the sample after post-gate RTA maintained a lower reverse-biased I_g even for $V_{gs} < -6$ V. It probably stems from the increased gate barrier height after Ni reaction with Al_2O_3 during the post-gate RTA.

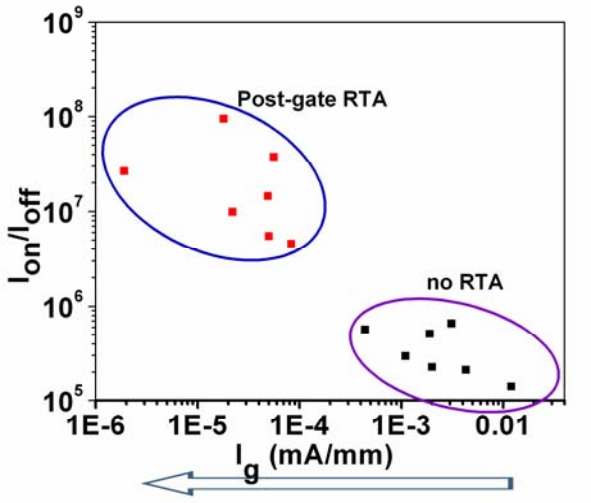

Figure 5 Correlation between I_{on}/I_{off} and gate leakage current. I_g was measured at V_{gs} = -8 V from the gate-source *I-V* characteristics.

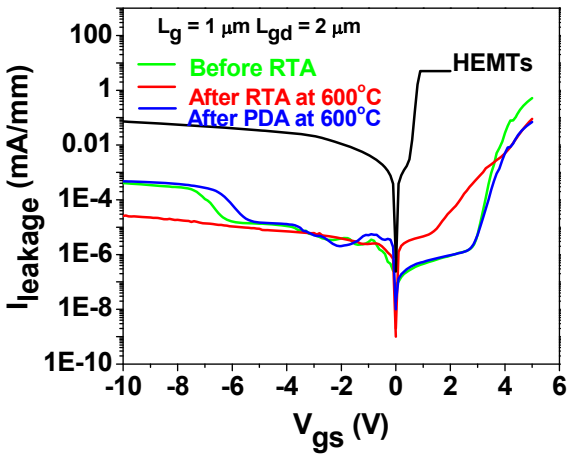

Figure 6 Comparison of gate leakage current of samples under three different thermal treatments: before RTA, post-gate RTA, and PDA.

Current collapse was also characterized with pulsed *I-V* measurements. A 0.5-ms pulse voltage was applied to the gate with base voltage kept at -16 V. However, the sample after post-gate RTA exhibited degraded pulsed *I-V* characteristics (Fig. 7(b)). This degradation may be due to some defect formation during RTA at 600 °C. In an attempt to recover the original characteristics, another post-gate RTA at 400 °C for 10 minutes was further performed. For samples underwent post-gate RTA at 600 °C for 10 seconds plus 400 °C for 10 minutes, the pulsed current could be mostly recovered (Fig. 7(c)) and the I_{off} was also retained low (Fig. 8).

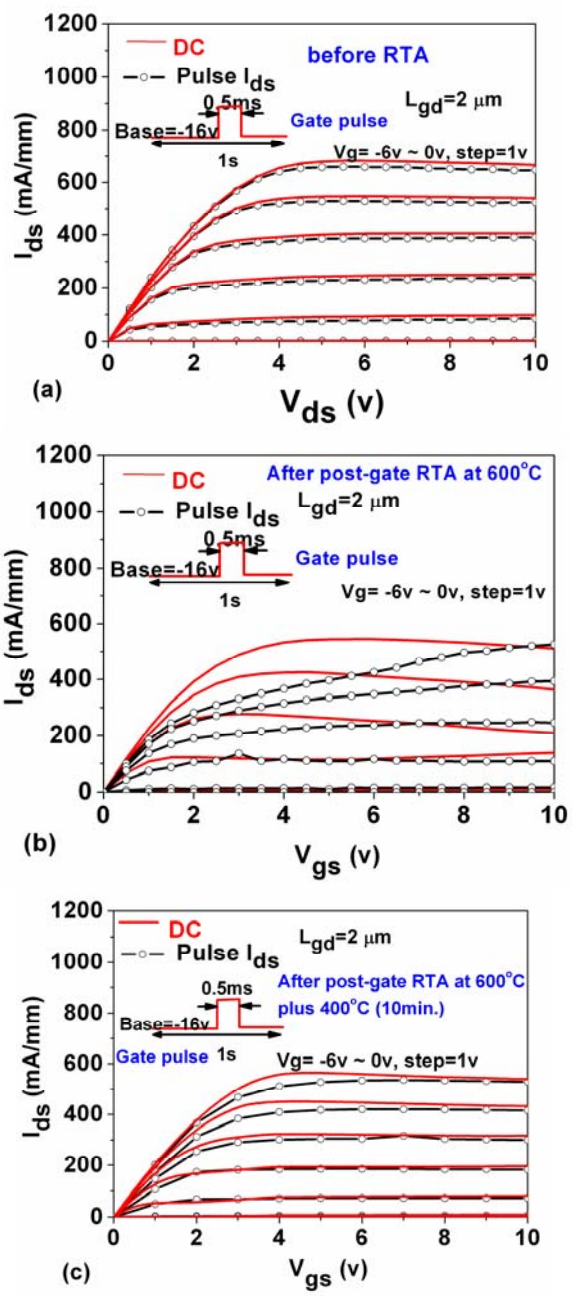

Figure 7 Pulsed *I-V* characteristics of samples: (a) before RTA, (b) after post-gate RTA at 600 °C, and (c) after post-gate RTA at 600 °C and another RTA at 400 °C for 10 minutes.

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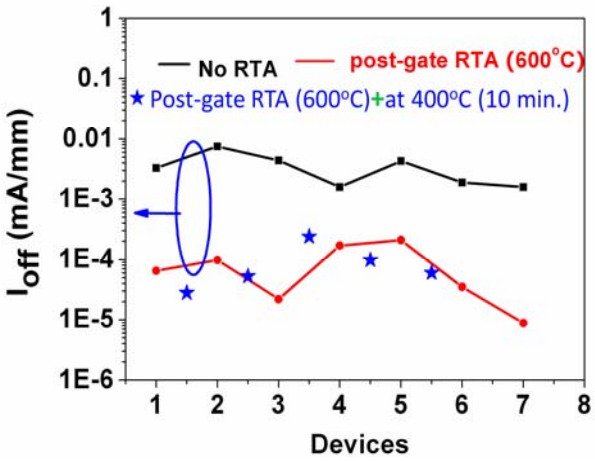

Figure 8 I_{off} of three kinds of samples: before RTA, after post-gate RTA at 600 °C, and after post-gate RTA at 600 °C plus another RTA at 400 °C for 10 minutes.

4 Conclusion

I_{off} in GaN MOSHEMTs was successfully reduced by more than one order of magnitude after post-gate RTA at 600 °C, for 10-30 seconds. Meanwhile, the I_{on}/I_{off} could be increased to around 10^7-10^8. The proposed mechanism resulting in this phenomenon is the increased barrier height after post-gate RTA. Defect induced during post-gate RTA at 600 °C could be greatly recovered by further post-gate RTA at 400 °C for 10 minutes.

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