Fabrication of 100-nm Metamorphic AlInAs/GaInAs HEMTs Grown on Si Substrates by MOCVD

Ming Li, Haiou Li, Chak Wah Tang, and Kei May Lau, *Fellow, IEEE*

***Abstract*—High-performance metamorphic $Al_{0.49}In_{0.51}As$-/$Ga_{0.47-}In_{0.53}As$ high-electron-mobility transistors (mHEMTs) grown on Si substrates by metal–organic chemical vapor deposition (MOCVD) using an effective multistage composite buffer scheme have been fabricated. Room-temperature Hall measurements show an average sheet carrier density of 4.5×10^{12} cm^{-2} with a mobility of over 7500 $cm^2/V \cdot s$. Maximum transconductance of mHEMTs with a 100-nm gate length was ~770 mS/mm, which is nearly the same as that of mHEMTs with the same dimension grown on GaAs substrates by MOCVD. The unity current gain cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) were 210 and 146 GHz, respectively. To our best knowledge, these results are the best reported for MOCVD-grown mHEMTs on Si.**

***Index Terms*—AlInAs/GaInAs, metal–organic chemical vapor deposition (MOCVD), metamorphic high-electron-mobility transistors (mHEMTs), silicon.**

I. Introduction

GaInAs channel metamorphic high-electron-mobility transistor (mHEMT) is one of the most promising device candidates for future high-speed and low-power digital logic applications [1], [2]. When benchmarked against state-of-the-art silicon MOSFETs, mHEMTs exhibited more than an order of magnitude improvement in energy-delay product, confirming their potential for ultrahigh-speed low-power logic applications [3]. However, there remain several significant challenges before practical implementation of III–V materials for logics [4], including integration of III–V heterostructures with the Si substrate. Seamless robust heterogeneous integration of high-performance GaInAs transistors on Si will help realize the ultimate vision of low-voltage high-speed III–V-based logic circuit blocks coupled with the functional density advantages provided by the Si CMOS.

Outstanding performance of mHEMTs on Si grown by molecular beam epitaxy (MBE) has been achieved, with device results comparable to HEMTs grown on GaAs or InP substrates [5], [6]. However, demonstration of mHEMTs on Si grown by metal–organic chemical vapor deposition (MOCVD) has lagged behind, although MOCVD has commercial manufacturing advantages. The inherent differences of the two growth techniques render more challenging issues in growing transistor structures by MOCVD. The metamorphic layer structures (lattice-matched to InP) grown on Si substrates by MOCVD have been characterized and demonstrated for the first time by our group [7]. Based on this previous study, we further improve the crystalline quality and surface morphology and reduce the buffer leakage by fine tuning the buffer layers. With better surfaces, high-frequency performance can be realized with the fabrication of 100-nm-gate-length mHEMTs.

In this letter, an optimized multistage LT/HT (low temperature/high temperature) GaAs/InP/AlInAs composite buffer layer (< 1.7 μm) with a thin GaInAs strained layer is introduced, which can improve the heterostructure material quality and surface morphology, thereby enhancing the RF performance. mHEMTs with a 100-nm gate length were fabricated using a combination of e-beam and photolithography. Both dc and RF performance of the fabricated AlInAs/GaInAs mHEMTs are evaluated.

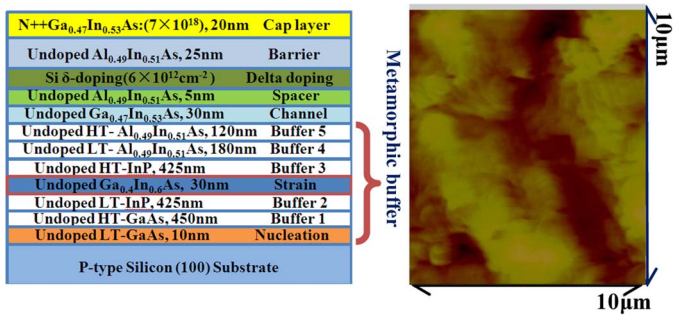

Fig. 1. Nominal structure of an mHEMT device on a Si substrate and an AFM image of 10×10 μm^2 scan area of buffer structures on a Si substrate.

II. Materials Growth and Device Fabrication

$Al_{0.49}In_{0.51}As/Ga_{0.47}In_{0.53}As$ mHEMTs lattice-matched to InP were grown on 4-in exact-(001) oriented p-type Si substrates using an Aixtron AIX-200/4 MOCVD system. The detailed epitaxial structure design, including five-stage composite buffers, is shown in Fig. 1.

From top to bottom, the epitaxial layer structure consists of a heavily doped (Si, 7×10^{18} cm^{-3}) 20-nm $Ga_{0.47}In_{0.53}As$ cap layer, a 25-nm undoped $Al_{0.49}In_{0.51}As$ barrier layer, Si-delta-doping, a 5-nm undoped $Al_{0.49}In_{0.51}As$ spacer layer, a 30-nm $Ga_{0.47}In_{0.53}As$ channel, a 120-nm HT-$Al_{0.49}In_{0.51}As$ layer (buffer 5 in Fig. 1), a 180-nm LT-$Al_{0.49}In_{0.51}As$ layer

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The authors are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Kowloon, Hong Kong (e-mail: eekmlau@ust.hk).

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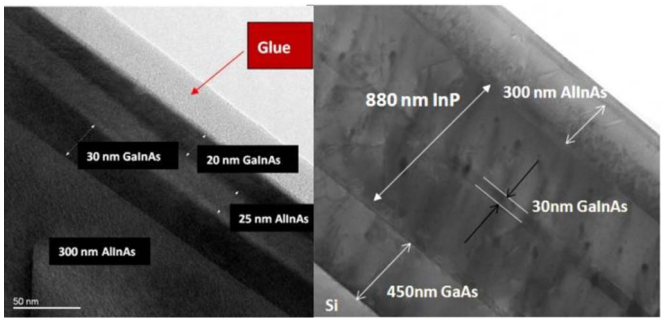

Fig. 2. TEM cross section micrograph of an mHEMT structure.

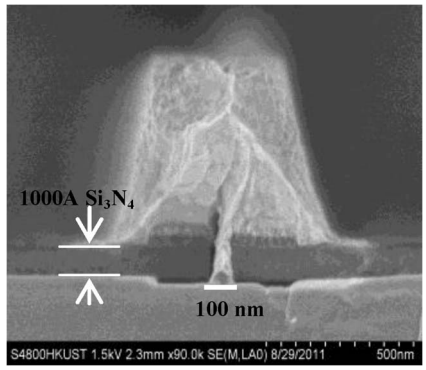

Fig. 3. Cross-sectional SEM graph of a T-shaped gate.

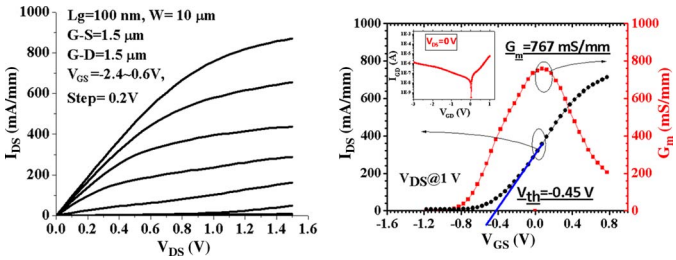

Fig. 4. DC IV–V characteristics and transfer characteristics of a $0.1 \times 10\ \mu\text{m}^2$ mHEMT.

III. DC Characteristics

After removal of the cap layer, room-temperature (RT) Hall measurements showed a 2DEG density of 4.5×10^{12} cm^{-2} with a mobility of 7500 cm^2/V $\cdot$ s at 300 K and 3×10^{12} cm^{-2} with a mobility of 23 000 cm^2/V $\cdot$ s at 77 K. These values are also comparable to that of similar structures grown on Si substrates by MBE [5].

The dc current–voltage characteristics of a 100-nm-gate-length AlInAs/GaInAs mHEMT on Si are shown in Fig. 4. The maximum measured drain current was about 860 mA/mm at $V_{GS} = 0.6$ V and $V_{DS} = 1.5$ V. The maximum extrinsic transconductance was 767 mS/mm at $V_{GS} = 0$ V and $V_{DS} = 1.0$ V. The device is a depletion-mode transistor with a threshold voltage V_{th} of around -0.45 V. The drain current below threshold was less than 0.32 mA/mm at $V_{GS} = -1.2$ V and $V_{DS} = 1.0$ V. The gate leakage current of the mHEMT was shown in the inset in Fig. 4. The reverse gate current is about 0.12 mA/mm at $V_{GS} = -3$ V and $V_{DS} = 1.0$ V, which is one order of magnitude lower than our previous work [7], showing the effectiveness of the higher resistivity multistage buffer layers.

IV. RF Performance

On-wafer S-parameter measurements were carried out on $0.1 \times 100\ \mu\text{m}^2$ mHEMTs using Cascade Microtech probes and an HP8722 network analyzer from 0.1 to 39.1 GHz. Open on-wafer deembedding structures were used to determine the parasitic capacitance of the probe pads and to deembed the short-circuit current gain $|h_{21}|$.

As shown in Fig. 5, the cutoff frequency f_T is about 210 GHz from the extrapolation of $|h_{21}|$ to unity using a

(buffer 4), a 425-nm composite HT-InP layer (buffer 3) grown at 600 °C, a 30-nm thin $Ga_{0.4}In_{0.6}As$ strained layer, a 425-nm low-temperature (LT) InP layer (buffer 2) grown at 500 °C, a 450-nm HT-GaAs layer (buffer 1), and a 10-nm GaAs nucleation layer. The lightly compressively strained thin 30-nm $Ga_{0.4}In_{0.6}As$ layer was inserted between the HT- and LT-InP to balance the overall strain in the composite buffer structure. According to high-resolution X-ray diffraction measurement, the full width half maximum of the GaAs and InP buffers are around 328 and 320.3 arcsec, respectively. These values indicate a good crystalline quality that is desirable for good device performance.

Fig. 1 shows the atomic force microscope image of the effective composite buffer surface morphology, demonstrating a smooth surface with rms roughness of around 2.5 nm across a scanned area of $10 \times 10\ \mu\text{m}^2$, which is slightly rougher than that of similar structures grown on GaAs substrates [8].

Fig. 2 shows the cross-sectional TEM images of the whole composite buffer layers. The 30-nm $Ga_{0.4}In_{0.6}As$ layer effectively balances the residue strain in the composite buffer, which is presumably fully relaxed to the lattice constant of InP. There are only few misfit dislocations, and 60-degree threading dislocations were confined in the buffer. After removing the active layers from the top of the sample with selective chemical wet etching, the sheet resistance of multistage buffer layers was measured to be larger than $10^4\ \Omega$/square from Hall measurements.

The devices were fabricated with mesa isolation and a six-layer metal system (Ni/Ge/Au/Ge/Ni/Au) for ohmic contacts. Transmission line measurements indicate that the nonalloyed ohmic contact resistance R_c was as low as 0.07 $\Omega \cdot$ mm. T-gate devices (100 nm) with 3-μm spacing between the source and the drain were fabricated by a two-stage electron beam lithography. L_{side} is about 120 nm. SiN_x (100 nm) films deposited by PECVD were used to define the gate footprint and mechanically support the T-shaped gate. After etching the SiN_x film using $CHF_3/CF_4/O_2$ reactive ion etching, the gate-head pattern was formed by a bilayer polymethylmethacrylate/polymethylglutarimide (PMMA/PMGI) process. The high-selectivity succinic-acid-based etchant was used to remove the highly doped GaInAs cap layer in order to stack T-shaped gates on the AlInAs barrier layer. Finally, Ti/Pt/Au was deposited as the Schottky gate contact. Fig. 3 shows a cross-sectional SEM photograph of 100-nm-gate-length T-shaped mHEMTs with a 400-nm-wide head.

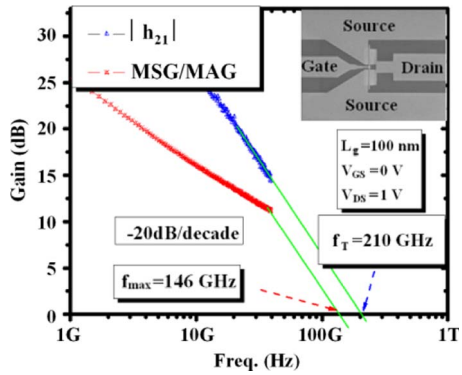

Fig. 5. Cross-sectional SEM graph and current gain MSG/MAG as a function of frequency of a 0.1 × 100 μm^2 T-shaped gate mHEMT.

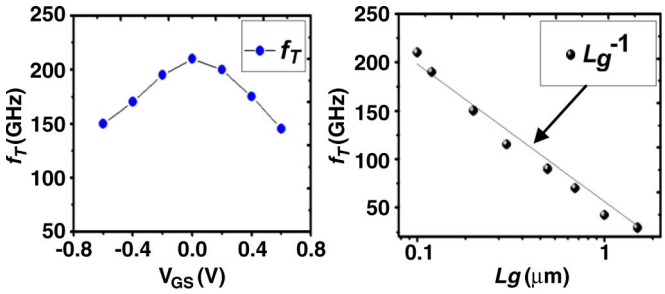

Fig. 6. Dependence of f_T on gate bias and gate length (L_g) for our mHEMTs, where V_{DS} is fixed at 1.0 V.

TABLE I
COMPARISON OF ALINAS/GAINAS HEMT PERFORMANCE

Hetero-structure	Sub.	Growth	Mob.	Lg (nm)	Gm (mS /mm)	f_T (GHz)	f_{max} (GHz)	Date	Ref.
$In_{0.52}AlAs/In_{0.53}GaAs$	GaAs	MBE	N/A	100	750	154	300	2004	[9]
$In_{0.52}AlAs/In_{0.53}GaAs$	GaAs	MBE	9100	150	750	140	240	2003	[10]
Al $In_{0.50}As/GaIn_{0.53}As$	Si	MOCVD	4540	1μm	587	32	44	2008	[7]
$In_{0.7}GaAs/In_{0.52}AlAs$	Si	MBE	10000	80	1200	302		2010	[6]
Al $In_{0.51}As/GaIn_{0.53}As$	Si	MOCVD	7500	100	767	210	146	2011	This work

−20-dB/dec slope, which is the highest value reported for mHEMTs on a Si substrate by MOCVD [7]. The maximum oscillation frequency $f_{\max}$ was about 146 GHz from the extrapolation of maximum stable gain/maximum available gain (MSG/MAG). Using equivalent circuit modeling of the measured 10–30-GHz S-parameters, a voltage gain (g_m/g_o) of 6.7 and an input capacitance to a gate-drain feedback capacitance ratio (C_{gs}/C_{gd}) of 3.1 were obtained, both of which are mainly responsible for the degradation of $f_{\max}$ in our mHEMTs. The dependence of f_T on gate bias (V_{GS}) and L_g are shown in Fig. 6. f_T of the 100-nm device did not show serious variation at both low and high gate biases [see Fig. 6(a)], indicating a good linearity. The inverse relationship of f_T and L_g is typical [see Fig. 6(b)].

Table I shows a comparison of different AlIn-As/GaInAs HEMTs, grown by MBE or MOCVD on GaAs or Si substrates and fabricated with similar gate lengths. The dc performance of mHEMTs on Si grown by MOCVD is comparable to that of HEMTs grown by MBE. Improved fabrication will enhance the RF characteristics as well in the future. These results are very encouraging toward the manufacturing of high-performance metamorphic devices on Si substrates by MOCVD.

V. CONCLUSION

In conclusion, submicrometer AlInAs/GaInAs mHEMTs grown on silicon substrates by MOCVD have been successfully fabricated. In these high-quality $Ga_{0.47}In_{053}As$ channel structures, the total thickness of the composite metamorphic buffer was less than 1.7 μm, and the buffer effectively accommodates the lattice mismatch between the mHEMT devices and the silicon substrate. A 100-nm-gate-length depletion-mode mHEMT exhibits a saturated peak dc transconductance of 767 mS/mm and intrinsic f_T of 210 GHz at $V_{DS} = 1.0$ V and $V_{GS} = 0$ V. To our best knowledge, these results are the best reported for MOCVD-grown mHEMTs on Si and will be useful for high-frequency and high-speed applications.

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