

Low-Leakage-Current AlN/GaN MOSHFETs Using Al₂O₃ for Increased 2DEG

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Abstract—Metal-oxide-semiconductor heterostructure field effect transistors (MOSHFETs) were fabricated with an AlN/GaN heterostructure grown on Si substrates. A 7-nm Al₂O₃ serving as both gate dielectric under the gate electrode and passivation layer in the access region was used. It was found that the Al₂O₃ was superior to SiN_x in increasing the 2-D electron gas (2DEG) density and thereby reducing the access resistance. In addition, the OFF-state leakage current (I_{off}) in these AlN/GaN MOSHFETs was reduced by four orders of magnitude to 7.6×10^{-5} mA/mm as a result of the Al₂O₃ gate dielectric, compared to that of AlN/GaN HFETs. Meanwhile, the subthreshold slope was improved to a nearly ideal value of 62 mV/dec because of the extremely low I_{off} . The MOSHFETs with 1- μm gate length exhibited good DC characteristics. A maximum drain current of 745 mA/mm and a peak extrinsic transconductance of 280 mS/mm were achieved.

Index Terms—AlN, Al₂O₃ passivation, GaN, heterostructure field effect transistors (HFETs).

I. INTRODUCTION

THIN AlN barrier offers the greatest scalable potential among different Al_xGa_{1-x}N alloy compositions because of its relatively large band gap and strong polarization effects. This can help improve the aspect ratio of HFETs and thus reduce the limitation of short channel effects on high-frequency operation. Despite such merits, it is difficult to grow high-quality AlN layers due to the existence of large tensile strain between the lattice-mismatched GaN and AlN (about 2.4%). Recently, outstanding performance of AlN/GaN HFETs grown by molecular beam epitaxy has been successfully demonstrated [1]–[6], including a peak transconductance of 700 mS/mm [3], a unity current gain cutoff frequency f_T of 220 GHz, and a unity power gain frequency f_{max} of 400 GHz [5]. However, limited progress has been made on AlN/GaN transistors grown by metalorganic chemical vapor deposition (MOCVD), despite MOCVD is a more commonly used technique for GaN-based devices. The previously reported AlN/GaN HFETs could not completely pinch-off due to low quality of the AlN barrier layers [7]–[10]. Recently, AlN/GaN HFETs have been grown by MOCVD on Si substrates with *in situ* grown SiN_x cap

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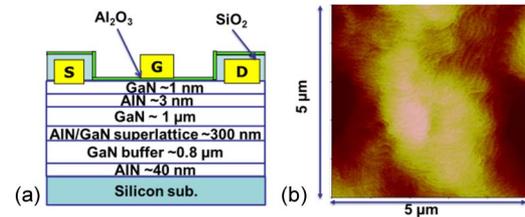


Fig. 1. Cross-sectional schematic of the AlN/GaN MOSHFETs (a), and AFM image of AlN surface (b).

layer for strain relaxation and increase of the 2-D electron gas (2DEG) density [11]–[13]. The SiN_x in the source/drain region must be selectively etched for ohmic contact formation. The reported I_{off} was still larger than 10^{-3} mA/mm. For high-performance RF power amplifiers, lower leakage current is more desirable, to avoid additional noise generation during transistor operation.

In this paper, an AlN/GaN heterostructure was grown on Si substrates by MOCVD for HFETs fabrication. We found that Al₂O₃ deposited by atomic layer deposition (ALD) is a more effective passivation dielectric than SiN_x, with additional benefit of increasing the 2-DEG density in AlN/GaN HFETs. ALD technology has been widely used in III-nitride MOSHFETs for the gate dielectric [1], [14]–[16]. However, limited work was focused on the passivation effect of high- k Al₂O₃. In this paper, we report AlN/GaN MOSHFETs fabricated with Al₂O₃ serving simultaneously as gate dielectric and passivation layer showing salient features such as low OFF-state current and reduced access resistance. The fabricated MOSHFETs exhibited an extremely low I_{off} of 7.6×10^{-5} mA/mm at $V_{\text{gs}} = -5$ V.

II. MATERIAL GROWTH AND DEVICE FABRICATION

The AlN/GaN heterostructure was grown on a Si (111) substrate by MOCVD. Fig. 1(a) shows the cross-sectional schematic of the GaN (1 nm)/AlN (3 nm)/GaN MOSHFETs with a 7-nm Al₂O₃ as gate dielectric and passivation. The epilayer thicknesses were estimated based on calibrated growth rates. The epitaxial structure consisted of, from bottom to top, a 40-nm AlN nucleation layer, an 800-nm GaN buffer layer, AlN(6 nm)/Al_{0.19}Ga_{0.81}N(28 nm) super-lattice interlayer with a total thickness of 300 nm for strain relaxation, a 1000-nm GaN layer, and a 3-nm AlN barrier layer. Finally, a 1-nm GaN protective layer was grown as cap. Fig. 1(b) is an atomic force microscopy (AFM) image of the as-grown sample surface, which is smooth with a clear atomic step structure. Dark defects, representing the intersection of threading dislocation, are not in high density. The root mean square roughness measured across the 5 $\mu\text{m} \times 5 \mu\text{m}$ scan was 0.6 nm. Room-temperature (RT) Hall measurements showed a 2-DEG density of

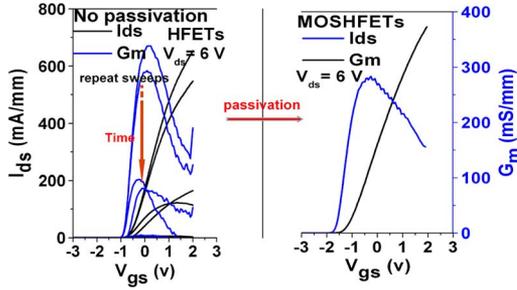


Fig. 2. Continuously repeated sweep measurements of transfer curve of HFETs (no passivation) and MOSHFETs (Al_2O_3 as passivation and gate dielectric). The drain-gate spacing (L_{gd}) is $1 \mu\text{m}$.

$1.44 \times 10^{13}/\text{cm}^2$ with a mobility of $1050 \text{ cm}^2/\text{V} \cdot \text{s}$, leading to a sheet resistance of $415 \Omega/\text{sq}$ at RT.

The AlN/GaN MOSHFETs fabrication process flow was as follows. Mesa isolation was performed using Cl_2/He plasma dry etching in an inductively coupled plasma reactive ion etching system. After patterning by optical lithography, source and drain electrodes with metal system Ti/Al/Ni/Au were deposited, followed by lift off and rapid thermal annealing (RTA) at 850°C for 30 s in nitrogen ambient. Before the deposition of Al_2O_3 by ALD, a layer of SiO_2 was coated using plasma-enhanced chemical vapor deposition (PECVD) to protect the ALD chamber from contamination by the source/drain metals. Then, the SiO_2 over the active region between source and drain contacts was removed by buffered oxide etchant solution for Al_2O_3 deposition. Pre-ALD treatment was with diluted HCl solution for 5 min. The amorphous Al_2O_3 was deposited at 300°C using trimethylaluminum and H_2O as precursors with ten cycles of H_2O pretreatment. Finally, the gate metal (Ni/Au) was deposited. All the measurements in this experiment were performed on transistors with $1\text{-}\mu\text{m}$ gate length (L_g) and $1\text{-}\mu\text{m}$ source-gate spacing (L_{gs}).

III. RESULTS AND DISCUSSION

In AlN/GaN HFETs, surface passivation is essential for the transistor performance. This is because the ultrathin AlN barrier layer makes the 2-DEG particularly sensitive to surface states. AlN/GaN HFETs without any surface passivation layer were also fabricated for comparison in this study. The drain current of this unpassivated AlN/GaN HFET was observed to decrease gradually when repeated sweeping of the transfer characteristics was made [Fig. 2 (left)]. Finally, the values of both the drain current and transconductance decreased to immeasurable levels. This phenomenon is caused by the surface trap centers, which trap electrons from channel/gate current during measurement with a very long time constant. When we continuously repeat the sweeping measurement, the trapped electrons do not have enough time to be released. As a result, more and more trapped electrons accumulated in the AlN surface, and thus increased the surface potential. The 2-DEG underneath the AlN layer was gradually depleted by the increased surface potential. We found that this degradation phenomenon could be completely eliminated by adding an Al_2O_3 passivation layer on the transistor surface. The Al_2O_3 layer in the AlN/GaN HFETs acted simultaneously as a gate dielectric and a surface passivation layer. In the case of AlN/GaN MOSHFETs, there was no current degradation when sweeping measurement was

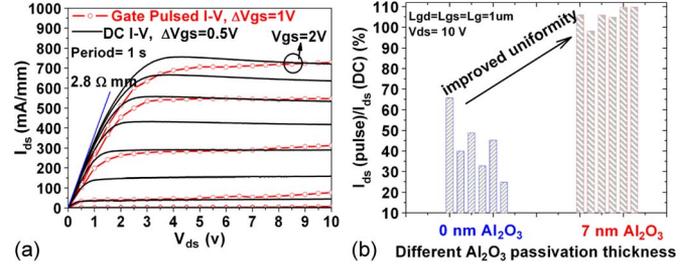


Fig. 3. (a) Output characteristics of gate pulsed I-V and DC I-V measurements in AlN/GaN MOSHFETs. (b) Histograms of $I_{ds}(\text{pulse})/I_{ds}(\text{DC})$ ratios at $V_{gs} = 2 \text{ V}$ of AlN/GaN HFETs and MOSHFETs.

continuously made [Fig. 2 (right)]. The Al_2O_3 passivation layer could eliminate the surface trapping effect and improve the transistor performances. In our experiment, this phenomenon of current degradation also disappeared as the AlN/GaN HFETs was passivated with SiN_x deposited by PECVD.

DC-RF dispersion of both MOSHFETs and HFETs were also characterized to verify the effectiveness of Al_2O_3 passivation. A $500\text{-}\mu\text{s}$ pulse voltage was applied to the gate with base voltage at -4 V (quiescent bias at pinch-off condition). Little current degradation in Fig. 3(a) shows good surface passivation effect of the 7-nm -thick Al_2O_3 in the access region. At higher drain bias, the pulsed I_{ds} shows a slightly higher current than DC I_{ds} , which probably arises from the interplay between self-heating during measurement and trap states [1]. However, in the case of unpassivated AlN/GaN HFETs, the pulsed I_{ds} decreases significantly compared with the DC I_{ds} , as shown by ratios of $I_{ds}(\text{pulse})/I_{ds}(\text{DC})$ in Fig. 3(b) of a number of devices. Moreover, the Al_2O_3 also dramatically improves the uniformity, also shown in the $I_{ds}(\text{pulse})/I_{ds}(\text{DC})$ plots, as the 2-DEG is rather sensitive to the surface condition. The results demonstrate the effectiveness of Al_2O_3 in the access region, as passivation to improve the ultrathin AlN barrier in enhancing the MOSHFET's performance.

From the DC current-voltage ($I_{ds}-V_{ds}$) curves in Fig. 3(a), a low ON-state resistance (R_{on}) of $2.8 \Omega \cdot \text{mm}$ was estimated. From the transmission line model structures, the ohmic contact resistance (ρ_c) was determined to be $0.34 \Omega \cdot \text{mm}$, and a low specific contact resistance of $3.7 \times 10^{-6} \Omega \cdot \text{cm}^2$ was obtained. The low ρ_c was realized by RTA at 850°C without any other optimization means. The reason may be due to the ultrathin AlN layer (3 nm) and high 2-DEG density ($1.44 \times 10^{13} / \text{cm}^2$) in our heterostructure.

In addition, the Al_2O_3 layer also effectively increases the 2-DEG density, which was demonstrated by the enhanced I_{ds} between the source and drain contacts with different Al_2O_3 thickness [Fig. 3(a)]. A 7-nm Al_2O_3 could induce more channel electron density than a 15-nm SiN_x deposited by PECVD. It was confirmed that the Al_2O_3 is a better candidate for passivation than SiN_x . With increasing Al_2O_3 thickness, the I_{ds} increased correspondingly but gradually saturated after the Al_2O_3 thickness is 15 nm and larger [Fig. 4(a)]. The different slope of saturated current in the case of SiN_x and Al_2O_3 passivation can also be explained by the different surface scattering effects, because the current is a strong function of electron mobility. From Hall measurement results [Fig. 4(b)], the measured 2-DEG density (N_s) of samples with 7-nm Al_2O_3 shows a very large increase compared with the samples without Al_2O_3 deposition. However, there is only a small increase

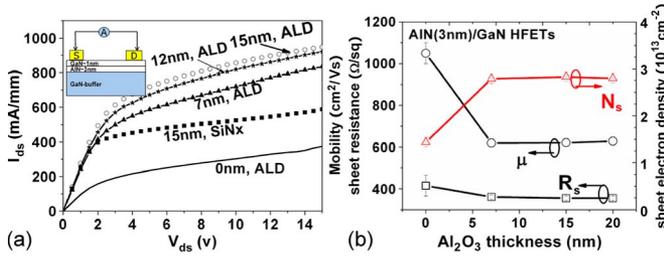


Fig. 4. (a) I_{ds} - V_{ds} characteristics between the source and drain terminals with Al_2O_3 and SiN_x passivation. The inset shows the measured schematic with 3- μm source-drain spacing. (b) Hall data of AIN (3 nm)/GaN heterostructures as a function of Al_2O_3 thickness.

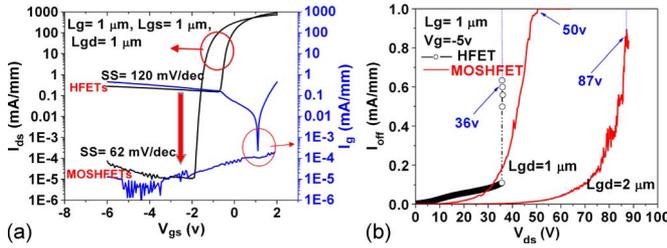


Fig. 5. (a) Semilog transfer curves of drain current and gate leakage current in HFETs and MOSHFETs. (b) Breakdown voltage curves of HFETs ($L_{gd} = 1 \mu\text{m}$) and MOSHFETs ($L_{gd} = 1 \mu\text{m}$ and $2 \mu\text{m}$) with $L_g = 1 \mu\text{m}$.

of N_s among samples with Al_2O_3 thicker than 7 nm. The proposed mechanism for the increased 2-DEG density is the positive charges in the dielectric/semiconductor interface and stress due to the deposited Al_2O_3 [17], [18]. The mobility drop after Al_2O_3 passivation may be a result of increased scattering among interfacial charges and electrons.

In the AIN/GaN MOSHFETs, the maximum drain current ($I_{d\text{max}}$) and peak extrinsic transconductance (G_m) were 745 mA/mm and 280 mS/mm at $V_{ds} = 6$ V, respectively [Fig. 2(b)]. The semilog transfer curves of MOSHFETs are also shown in Fig. 5(a). In comparison with a Schottky HFET, both the gate leakage and OFF-state drain leakage (I_{off}) decreased significantly in the MOSHFETs. The I_{off} decreased by four orders of magnitude from 2.5×10^{-1} to 7.6×10^{-5} mA/mm, and a high $I_{\text{on}}/I_{\text{off}}$ ratio of 10^8 was achieved. The I_{on} and I_{off} were measured at $V_{gs} = 2$ V and $V_{gs} = -5$ V, respectively. The I_{off} in the HFETs was primarily a result of gate leakage current tunneling through the ultrathin AIN barrier. The insertion of a layer of Al_2O_3 gate dielectric effectively reduced the gate leakage. Moreover, the subthreshold slope (SS) also decreased from 120 to 62 mV/decade in MOSHFETs, which was very close to the theoretical limit at 300 K. The improved SS obviously is also due to the large $I_{\text{on}}/I_{\text{off}}$ ratio in the MOSHFETs.

The OFF-state breakdown voltages (BV_{off}) were also assessed [Fig. 5(b)]. The BV_{off} of the AIN/GaN HFETs with $L_{gd} = 1 \mu\text{m}$ was 36 V. By inserting a layer of Al_2O_3 , the BV_{off} of the AIN/GaN MOSHFETs increased to 50 V for $L_{gd} = 1 \mu\text{m}$, and to 87 V for $L_{gd} = 2 \mu\text{m}$. The HFETs show low breakdown voltage with large leakage current. The introduction of Al_2O_3 could significantly reduce the leakage current, which is beneficial for increasing the breakdown voltage.

IV. CONCLUSION

MOSHFETs based on AIN/GaN heterostructure grown on Si substrates by MOCVD were fabricated. The Al_2O_3 deposited

by ALD acted simultaneously as a gate dielectric and a surface passivation layer. The Al_2O_3 passivation layer effectively eliminates the surface trap centers and increases the 2-DEG density due to the introduction of positive charge and stress. A maximum drain current of 745 mA/mm and peak G_m of 280 mS/mm were obtained in the AIN/GaN MOSHFETs with $L_g = 1 \mu\text{m}$. An extremely low I_{off} of 7.6×10^{-5} mA/mm and high $I_{\text{on}}/I_{\text{off}}$ ratio of 10^8 were realized in the MOSHFETs.

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