# InAlAs/InGaAs Metamorphic HEMT and MOS-HEMT with Regrown Source/Drain by MOCVD

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As scaling technologies are being stretched harder and harder in the roadmap of Si based CMOS, III-V compounds have become competitive alternative channel materials for the next generation high speed and low power transistors. Among various device structures, InGaAs HEMT has been intensively researched in the past few years because of its excellent carrier transport properties [1-3]. However, conventional HEMT structures requiring recessed gate technology may be difficult for digital VLSI applications due to their large footprint and higher parasitic capacitances [4]. Moreover, the gate recess process raises serious concerns in threshold voltage uniformity caused by variations in recess etching depth [5]. Selective Source/Drain (S/D) regrowth, which has been implemented in advanced Si pMOSFET, is an easier and scalable approach to facilitate ohmic contact in HEMT structures, with the benefits of eliminating reliability issues related to gate recess and parasitic reduction. In this paper, we describe the process and preliminary device results of metamorphic HEMTs (mHEMTs) and MOS-HEMTs on GaAs substrates with highly doped $In_{0.53}Ga_{0.47}As$ S/D by selective regrowth using MOCVD.

InAlAs/InGaAs metamorphic HEMT structures were grown on (100) oriented GaAs substrates in an Aixtron AIX-200/4 MOCVD system. Fig.1 shows the layered structure. From Hall measurements, an electron mobility of 7230cm$^2$/V·s with a sheet carrier density of $3.9 \times 10^{12}$/cm$^2$ at 300K was obtained. After the HEMT structure growth, a 1000 Å $SiO_2$ layer was used to pattern regions for S/D recesses etching down to the InGaAs channel layer. The sample was then loaded into the MOCVD system for $In_{0.53}Ga_{0.47}As$ regrowth in the etched regions at 670°C. Good selectivity was achieved. The $SiO_2$ mask was removed by BOE subsequently. An AFM image in the regrowth region is given in Fig.2, showing a rms value of 1.0 nm over a scanned area of 3×3 μm$^2$.

Both metamorphic HEMTs and MOS-HEMTs featuring regrown S/D were fabricated. Fig.3 lists the major process flow. Firstly, mesa isolation was formed by wet etching down to the InAlAs buffer. A 12nm thick $Al_2O_3$ was deposited by ALD for the MOS-HEMT sample after immediate pre-treatment using HCl:$H_2O$ (1:10) for 3mins. Non-alloyed S/D ohmic contacts were formed using a six-layer metal scheme (Ni/Ge/Au/Ge/Ni/Au). Finally, gate electrodes were defined by electron beam evaporation of Ti/Pt/Au and lift-off. Fig.4 illustrates the cross-sectional schematic of the devices after processing. From TLM measurements, a low specific contact resistivity of $1\times10^{-6}$ Ω·cm$^2$ was achieved for the non-alloyed S/D ohmic contacts. Fig.5 and Fig.6 show the output and transfer characteristics, respectively. 1-μm gate-length HEMT exhibits threshold voltage $V_T$ = -0.25 V, maximum drain current $I_{dss}$ = 168 mA/mm, and extrinsic peak transconductance $G_{max}$ = 302 mS/mm, while the MOS-HEMT shows $V_T$ = -3.8V, $I_{dss}$ = 186 mA/mm, and $G_{max}$ = 76 mS/mm. Fig.7 depicts gate leakage characteristics of both devices. The gate leakage for MOS-HEMT is five orders of magnitude lower compared with HEMT. Fig.8 illustrates the multi-frequency Capacitance-Voltage(C-V) response of MOS-HEMT. The sharp transition from accumulation to depletion region and the small frequency dispersion in the accumulation region indicate good $Al_2O_3$/InAlAs interface quality.

The DC performance of both HEMT and MOS-HEMT with regrown S/D is believed to be limited by the large Gate-to-Source separation $L_{GS}$ (1.5μm) and Gate-to-Drain separation $L_{GD}$ (1.5μm). In conventional HEMT structure, as shown in Fig.9, the access resistance in S/D-to-Gate region is dominated by the highly conductive n-InGaAs cap layer, which is small enough compared with the intrinsic channel resistance. However, for HEMT and MOS-HEMT featuring regrown S/D described in Fig.4, the current flows through 2DEG in S/D-to-Gate region, which results in a much larger access resistance. By minimizing $L_{GS}$ and $L_{GD}$, and further thinning the InAlAs barrier and ALD-$Al_2O_3$, improved performance of the regrown devices is expected.

**Reference:**

[1] D. H. Kim and J. A. del Alamo, IEDM Tech. Dig., 2006, pp. 837-840.
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[3] T.-W. Kim, D.-H. Kim, and J. del Alamo, IEDM Tech. Dig., 2009, pp. 483–486.
[4] S. Oktyabrsky and P. D. Ye, Fundamentals of III-V Semiconductor MOSFETs. New York: Springer, 2010.
[5] Iain Thayne *et al*, Electrochem. Soc. Transaction, vol.25, no.7, pp.385-389. 2009.

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|---|---|
| Undoped $In_{0.42}Al_{0.58}As$, 20nm, | Barrier |
| Si δ-doping, $4\times10^{12}/cm^2$ | Delta doping |
| Undoped $In_{0.42}Al_{0.58}As$, 5nm, | Spacer |
| Undoped $In_{0.6}Ga_{0.4}As$, 30nm, | Channel |
| Undoped HT- $In_{0.42}Al_{0.58}As$, 100nm | Buffer 5 |
| Undoped LT- $In_{0.45}Al_{0.55}As$, 200nm | Buffer 4 |
| Undoped HT- InP, 650nm | Buffer 3 |
| Undoped LT- InP, 110nm | Buffer 2 |
| Undoped GaAs, 100nm | Buffer 1 |
| Semi-Insulating GaAs substrate | |

**Fig.1.** mHEMT epitaxial layer structure

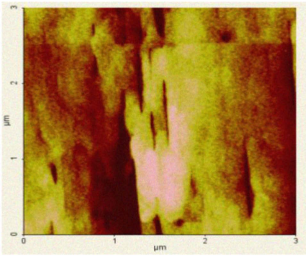

**Fig.2.** AFM image of the regrowth S/D

1000Å $SiO_2$ deposited by PECVD
$SiO_2$ etching in S/D region
S/D recess etching down to InGaAs channel
N+ InGaAs regrowth at 670°C
$SiO_2$ mask removal
Mesa isolation etching
ALD $Al_2O_3$ depostion
- pretreatment using 10% HCl for 3min
- 12nm-$Al_2O_3$ deposited at 300°C

S/D ohmic contact using Ni/Ge/Au/Ge/Ni/Au
Gate metallization using Ti/Pt/Au and lift-off

**Fig.3.** Process flow for mHEMT and MOS-HEMT. The only difference is that there is no ALD step in mHEMT

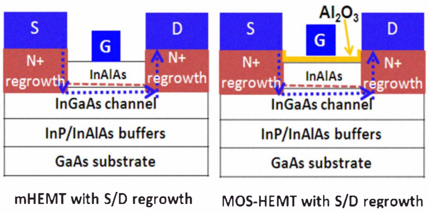


**Fig.4.** Schematic of mHEMT and MOS-HEMT. (blue dashed line: simplified drain current path)

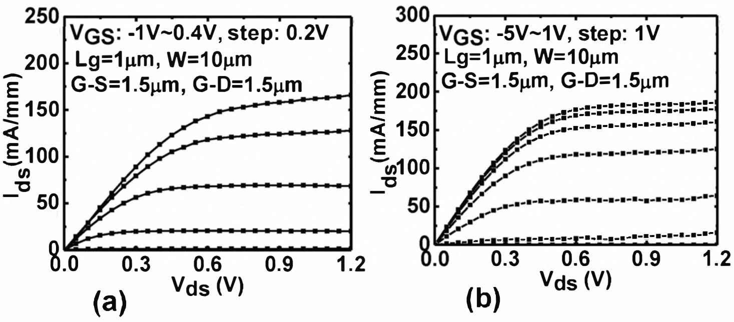


**Fig.5.** Output characteristics of mHEMT **(a)** and MOS-HEMT **(b)** with regrown S/D

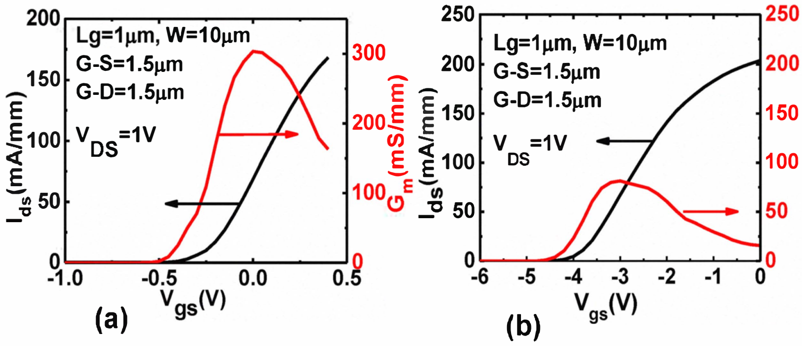


**Fig.6.** Transfer characteristics of mHEMT **(a)** and MOS-HEMT **(b)** with S/D regrowth

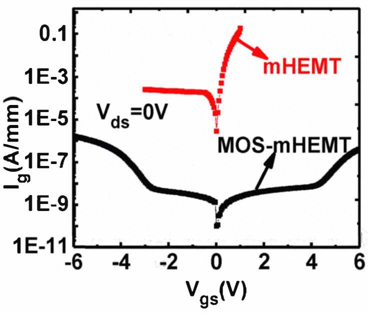


**Fig.7.** Gate leakage characteristics of mHEMT and MOS-HEMT

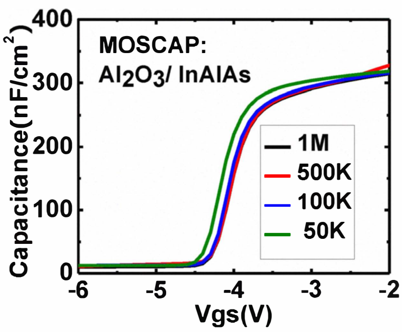


**Fig.8.** C-V curve of $Al_2O_3$/InAlAs interface for MOS-HEMT with regrown S/D

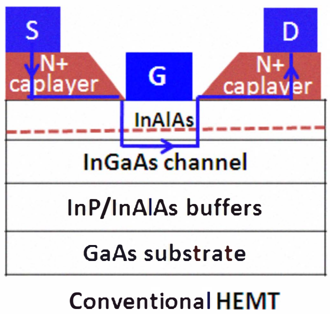


**Fig.9.** Schematic of conventional HEMT (blue lines: simplified drain current path)