InP Lattice-matched HEMT with Regrown Source/Drain by MOCVD

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Abstract

In this paper, we report the incorporation of Source/Drain regrowth by MOCVD in InAlAs/InGaAs HEMT on InP substrate. Greatly improved RF performance of the device was observed, compared with standard HEMTs with the same layered structure. 1-μm gate-length device exhibits a 34% improvement of cutoff frequency f_T and a 74% improvement of maximum oscillation frequency f_{max}.

1 Introduction

Since the implementation of 90nm technology node, selective epitaxy of SiGe Source/Drain (S/D) has been employed in advanced Si pMOSFET [1]. The compressively strained channel offers increased hole mobility, thus larger drive current. As Moore's Law is approaching fundamental limit, III-V high mobility channel transistors are promising candidates for the next generation high-speed and low-power logic applications [2, 3]. In the past few years, most of the research on III-V transistors has been focused on gate stack and considerable progress has been made. However, less attention was paid to S/D formation, which is critical in terms of achieving shallow S/D junction, low access resistance, and scalable device pitch.

Selective regrowth is an attractive technique among various S/D engineering methods. One major advantage lies on its capability in providing heavily doped S/D without severe crystal damage or any post-annealing as needed for ion implantation [4]. Heavily doped S/D can also result in reduced parasitic elements and low junction leakage, which is particularly important for scaled devices [5]. In traditional III-V transistors, biaxial-strain is usually applied intentionally to boost device performance. Recently, it is reported that, by introducing uni-axial stress in InGaAs MOSFET using lattice-mismatched S/D regrowth, electron mobility and drive current could be further improved [6]. Also, it is suggested by device simulation that the $In_{0.52}Ga_{0.48}As$ channel HEMTs featuring highly doped $In_{0.4}Ga_{0.6}As$ S/D regions would provide better DC and RF performance [7]. Therefore, selective regrowth is also a promising approach for strain engineering in device design.

In this paper, highly doped InGaAs S/D was incorporated in baseline InAlAs/InGaAs lattice-matched HEMTs using selective regrowth by MOCVD. Both DC and RF performance were measured and compared with standard InAlAs /InGaAs HEMTs fabricated with regular surface S/D and recessed gates.

2 Material Growth and Device Fabrication

InP lattice-matched HEMTs were grown using an Aixtron AIX-200/4 MOCVD with LayTec's EpiRAS in-situ monitoring system. Depicted in Fig.1, the HEMT structure starts with a 100nm un-doped InP buffer on a (1 0 0) oriented InP substrate. 200nm Low-Temperature (LT) InAlAs was grown at 525°C to achieve high resistivity, followed by 100nm High-Temperature (HT) InAlAs buffer grown at 670°C to ensure good crystalline quality. The device active layers on top consist of 30nm InGaAs channel, 5nm InAlAs spacer, 25nm InAlAs barrier and 15nm InGaAs cap. High Resolution XRD was used to determine the alloy compositions in the layers. All the layers are nearly compositional lattice-matched to InP. From Hall measurements, the InAlAs/InGaAs HEMT shows an electron mobility of 6080cm^2/V·s, with sheet carrier density of 3.8×10^{12}/cm^2 at 300K.

$In_{0.53}Ga_{0.47}As$: Si, $5 \times 10^{18}/cm^3$, 15nm,	Cap layer
Undoped $In_{0.56}Al_{0.44}As$, 25nm,	Barrier
Si δ-doping, $4\times10^{12}/cm^2$	Delta doping
Undoped $In_{0.56}Al_{0.44}As$, 5nm,	Spacer
Undoped $In_{0.53}Ga_{0.47}As$, 30nm,	Channel
Undoped HT- $In_{0.56}Al_{0.44}As$, 100nm	Buffer
Undoped LT- $In_{0.57}Al_{0.43}As$, 200nm	Buffer
Undoped InP, 100nm	Buffer
Semi-Insulating InP substrate	

Fig.1. Layered Structure of InAlAs/InGaAs HEMT

Fig.2 lists the major process steps. S/D recesses were etched down to the InGaAs channel by SiO_2 patterning. The sample was loaded into the MOCVD system after the S/D etching, without any other pre-treatment. Selective regrowth of n-$In_{0.53}Ga_{0.47}As$ at 670°C in the etched region was performed. Good selectivity of growth inside was achieved, using TMIn, TMGa, AsH_3, SiH_4 as precursors. The SiO_2 mask was removed by BOE subsequently. According to Hall measurements of planer n-InGaAs regrowth on samples without SiO_2 patterns, the Si doping concentration is estimated to be around $3\times10^{19}/cm^3$. The top view of one regrown HEMT before device fabrication is shown in Fig.3.

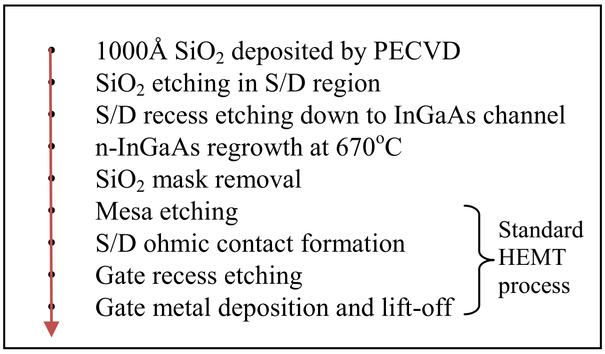

Fig.2 Process flow of HEMT with regrown S/D

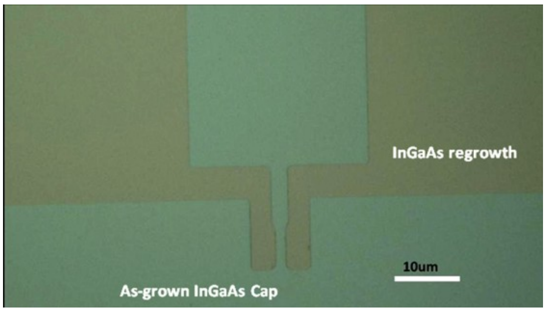

Fig.3 Microscope image of HEMT ($1\times 10\mu m^2$) after S/D regrowth and SiO_2 pattern removal

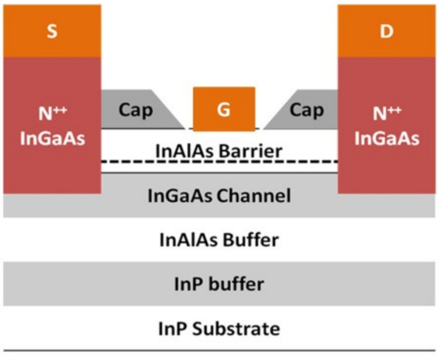

Fig.4 Cross-section of the HEMT with regrown S/D

To facilitate device comparison, a standard InP HEMT with a slightly higher carrier density ($4.6\times10^{12}/cm^2$) and better mobility ($6770cm^2/V{\cdot}s$) was also processed. 1-µm gate-length devices were fabricated. Firstly, mesa isolation was formed by wet etching down to the LT InAlAs buffer. Non-alloyed S/D ohmic contacts were formed using a six-layer metal scheme (Ni/Ge/Au/Ge/Ni /Au). Gate recess was formed using a succinic acid-based etchant to remove the n-InGaAs cap layer. Finally, gate metal was deposited as the Schottky contact by electron beam evaporation of Ti/Pt/Au and lift-off process. The spacing between gate-source and gate-drain were both 1.5 µm. Fig.4 illustrates the cross-section schematic of InP HEMTs with regrown S/D after process.

3 Results and Discussion

The specific contact resistivity (ρ_c) of non-alloyed S/D ohmic was measured using transmission-line matrix (TLM) technique. ρ_c was determined to be 1.4×10^{-6} $\Omega{\cdot}cm^2$ for the HEMT with regrown S/D, much lower than that of 2.4×10^{-5} $\Omega{\cdot}cm^2$ for standard HEMT. The lower ρ_c indicates a high doping level in the regrown InGaAs S/D.

Fig.5 and Fig.6 compare the output and transfer characteristics of $1\times 10\mu m^2$ gate devices. Both samples show excellent pinch-off and saturation characteristics. The HEMT with regrown S/D exhibits threshold voltage (V_T) = -0.85V, I_{Dsat} = 630mA/mm at V_{GS}=0.4V, peak Gm =501mS/mm, while the standard HEMT shows V_T= -0.9V, I_{Dsat} = 750 mA/mm at V_{GS}=0.4V, peak Gm=644 mS/mm. Fig.7 gives the gate leakage characteristics for the HEMT with S/D regrowth. The reverse-bias gate leakage current is I_{GS}= 0.05mA/mm at V_{GS}=-2V.

It was found that the access resistance of the HEMT with regrown S/D is not as good as the standard HEMT, despite of the lower contact resistivity measured. It might be a result of the yet to be optimized growth conditions for Si incorporation, or defects at the vertical regrowth interfaces.

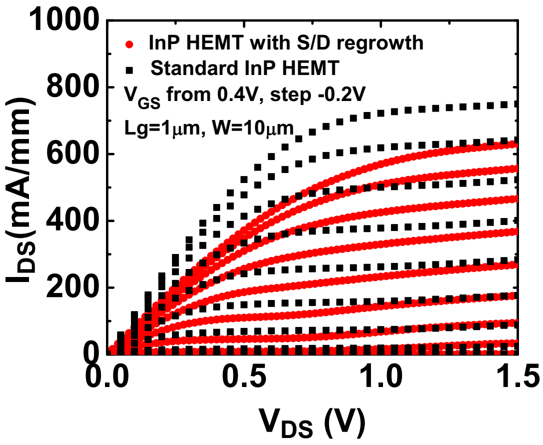

Fig.5 Output characteristics of InAlAs/InGaAs HEMT

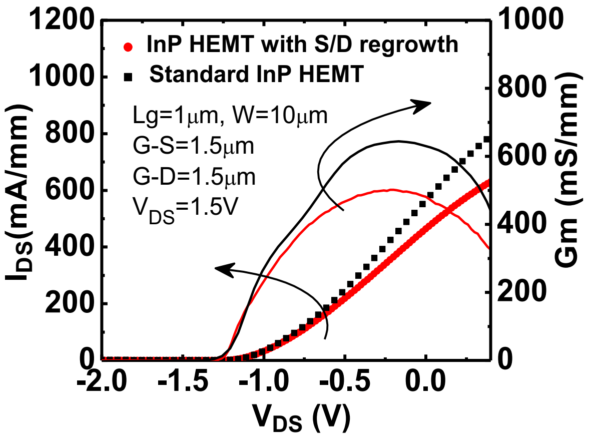

Fig.6 Transfer characteristics of InAlAs/InGaAs HEMT

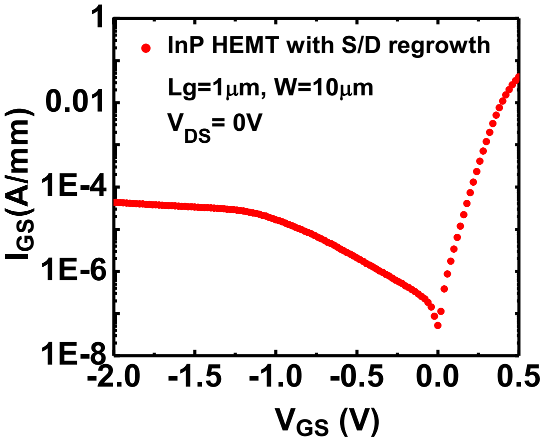

Fig.7 Gate leakage characteristic for the HEMT with regrown S/D

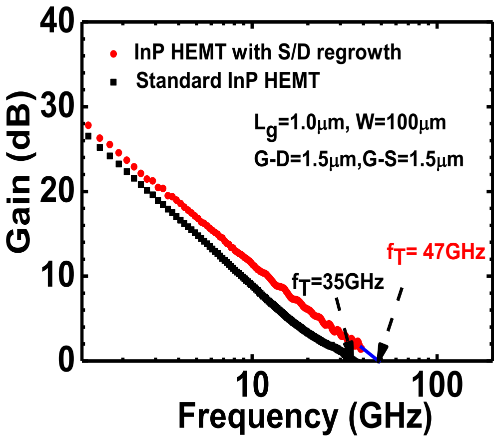

Fig.8 Current gain vs. frequency of 1× 100μm^2 gate HEMT

RF characteristics were compared for InAlAs/InGaAs HEMTs with a gate dimension of 1× 100μm^2. Fig.8 and Fig.9 present the measured current gain cutoff frequency f_T and the maximum oscillation frequency f_{max} at the maximum transconductance Gm, respectively. The InAlAs/InGaAs HEMT with regrown S/D exhibits f_T= 47GHz and f_{max}= 66GHz, while the referenced standard HEMT shows f_T= 35GHz and f_{max}=38GHz. It should be noted that the HEMT with regrown S/D demonstrates 34% and 74% improvement in f_T and f_{max}, respectively, although the extrinsic Gm is degraded. Gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd} were extracted from S-parameters at V_{GS} with maximum Gm. The HEMT with S/D regrowth shows C_{gs} =2.2pF/mm and C_{gd}=0.3pF/mm, much lower than that of standard HEMT (C_{gs}=4.2pF/mm, C_{gd}=0.32pF/mm). The drastically reduced C_{gs} and C_{gd} result in a higher ratio of transconductance to gate capacitance, leading to significantly boosted RF performance.

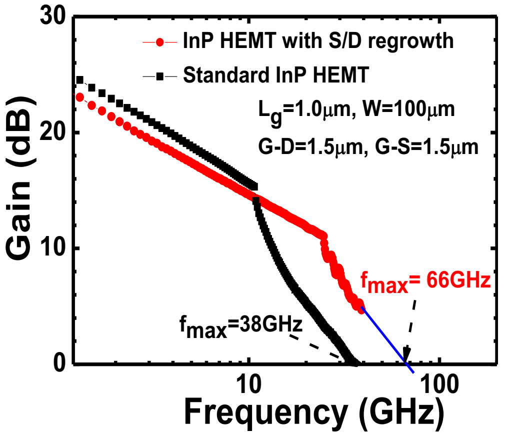

Fig.9 MSG/MAG vs. frequency of 1× 100μm^2 gate HEMT

4 Conclusion

InP lattice-matched HEMT with regrown S/D was experimentally demonstrated. Compared with our baseline 1-μm gate-length InAlAs/InGaAs HEMTs, f_T and f_{max} was improved by 34% and 74%, respectively. To fully explore the benefits of selective S/D regrowth in III-V transistors, optimization of both material growth and device structure is in progress.

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