InGaAs MOS-HEMTs on Si Substrates Grown by MOCVD

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Abstract

We present $In_{0.53}Ga_{0.47}As$-channel metal-oxide-semiconductor high electron mobility transistors (MOS-HEMTs) on Si substrates grown by metalorganic chemical vapor deposition (MOCVD) for the first time. Atomic-layer-deposited (ALD) Al_2O_3 was used as gate dielectric. A low-temperature process was developed to achieve good ohmic contact and maintain material integrity. A 1-μm gate-length device shows a maximum drain current of 415 mA/mm and extrinsic transconductance of 329 mS/mm. The gate leakage current is 7.3 nA/mm at gate bias of -3V, which is six orders of magnitude lower than that of the conventional HEMT using the same heterostructure.

1. Introduction

As scaling technologies are being stretched harder and harder in the roadmap of Si based CMOS, novel device architectures and new materials are being intensively explored [1-8]. InGaAs channel metamorphic high electron mobility transistor (mHEMT) is a promising candidate for high-speed low power logic application due to its excellent driving current performance at low voltages [9]. However, conventional HEMT devices with schottky-contact gates suffer from a large gate leakage current that is undesirable for the requirement of high on/off ratio for logic applications. To alleviate this problem, a high-k dielectric compatible with the InGaAs is necessary. In the quest for high-quality insulators with low interface state density on III-V materials in the past 40 years, recently significant progress has been made using *ex situ* ALD-Al_2O_3, HfO_2, ZrO_2 and *in situ* molecule-beam-epitaxial (MBE) $Ga_2O_3(Gd_2O_3)$ [10-13]. MOS-HEMTs not only reduce the gate leakage dramatically, but also have high channel mobility in the 2DEG.

As Si is the most common platform in the IC industry, it is more desirable to integrate the III -V MOS devices with Si technology. On the other hand, it is well known that III-V MOSFETs usually have low thermal tolerance in the device fabrication process. Degradation of the interface between the gate oxide and III-V materials after high-temperature process has been observed due to the As out-gasing from InGaAs and the inter-diffusion between Al_2O_3 and InGaAs [3,14]. For the III-V epitaxial layers grown on Si substrate, the large mismatch in thermal expansion coefficient also requires a low thermal processing.

In this paper, $In_{0.53}Ga_{0.47}As$-channel MOS-HEMTs grown on Si substrates by MOCVD were demonstrated for the first time. ALD-Al_2O_3 was employed to lower the gate leakage. A low temperature process has been developed to achieve low contact resistance as well as maintain material integrity. Good DC and RF characteristics are reported.

2. Device Structure and Fabrication

Fig.1 shows the schematic of the MOS-HEMT on Si substrate. The epitaxial layer structure was based on the metamorphic $In_{0.53}Ga_{0.47}As/In_{0.51}Al_{0.49}As$ heterojunction layers lattice-matched to InP. A 110-nm GaAs buffer, a 760-nm InP buffer, a 300-nm $In_{0.51}Al_{0.49}As$ buffer, a 18-nm undoped $In_{0.53}Ga_{0.47}As$ channel, a 5-nm $In_{0.51}Al_{0.49}As$ spacer, a 25-nm $In_{0.51}Al_{0.49}As$ barrier layer, and a 15-nm Si-doped $5\times10^{18}cm^{-3}$ $In_{0.53}Ga_{0.47}As$ cap layer were sequentially grown by MOCVD on 4-inch Si substrates. A silicon δ-doping layer with doping density of $4\times10^{12}cm^{-2}$ was placed above the channel.

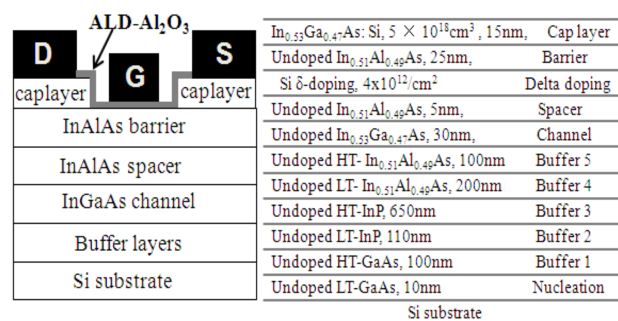

Fig.1. schematic of InGaAs MOS-HEMT on Si substrate

The fabrication process flow is illustrated in Fig.2. Firstly, mesa isolation was formed by wet chemical etching down to the low-temperature grown InAlAs buffer after surface cleaning. Then succinic acid/hydrogen peroxide solution was used to realize the gate recess. 15nm Al_2O_3 was deposited by ALD at 300˚C immediately after surface pretreatment in 10% HCl for 3min. After the removal of Al_2O_3 in the source/drain regions by buffered-oxide-etch (BOE), ohmic contacts were achieved by electron beam evaporation of a six-layer metal of Ni (40Å)/Ge(40Å)/Au(660Å)/Ge(80Å)/Ni(30Å)/Au(2500Å) and patterned by lift off process, followed by annealing at 280˚C for 10min by rapid thermal annealing (RTA) in N_2

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ambient. Finally the gate was made by the evaporation of Ti(200Å)/Au (2000Å) and lift off.

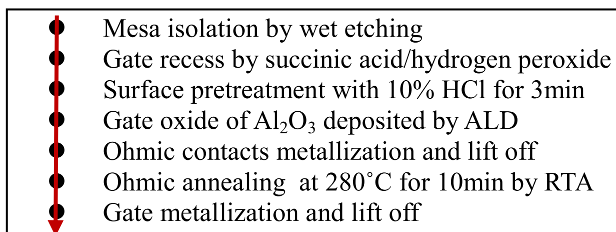

Fig.2. Fabrication process flow for MOS-HEMT

3. Results and Discussion

Fig.3 shows the output characteristic of the InGaAs MOS-HEMT on Si substrate with a gate bias from -1 to 1.4 V in steps of +0.4 V. For a typical 1um-gate length device, the maximum drain current (I_{dss}) was measured as 415 mA/mm at V_{gs} = 1.4 V and V_{ds} = 2 V. The on resistance was calculated to be 1578 Ω·µm from the I_{ds}-V_{ds} curve. Fig.4 shows the transfer characteristics at a drain bias of 1.5 V. A maximum extrinsic transconductance (G_{max}) of 329 mS/mm was achieved at V_{gs} = -0.1V. The gate leakage current characteristics of MOSHEMT and mHEMT using the same heterostructure are shown in Fig.5. The gate leakage current of MOS-HEMT was 7.3nA/mm at a gate bias of -3V, which was six orders of magnitude lower than that of the conventional mHEMT.

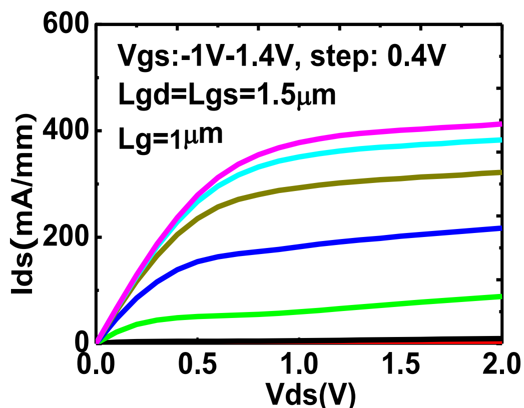

Fig.3. I_{ds}-V_{ds} characteristics of InGaAs MOS-HEMT.

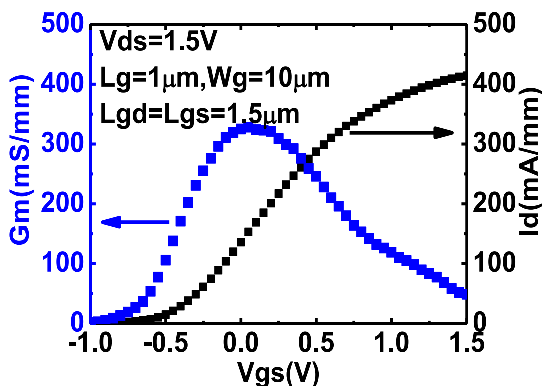

Fig.4. Transfer characteristics of MOS-HEMT on Si.

After ohmic contact annealing at 280˚C for 10 min in N_2 ambient by RTA, a low contact resistance of 0.13 Ω-mm and a sheet resistance of 224 Ω/sq were obtained from the transmission line measurement (TLM). Fig.6 shows the RF characteristics with a cut-off frequency of 18.6 GHz and a maximum oscillation frequency of 32.8 GHz.

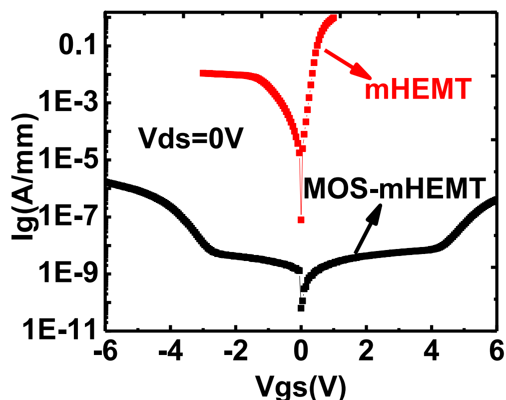

Fig.5. Gate leakage current of MOS-HEMT and mHEMT on Si substrate using the same heterostructure.

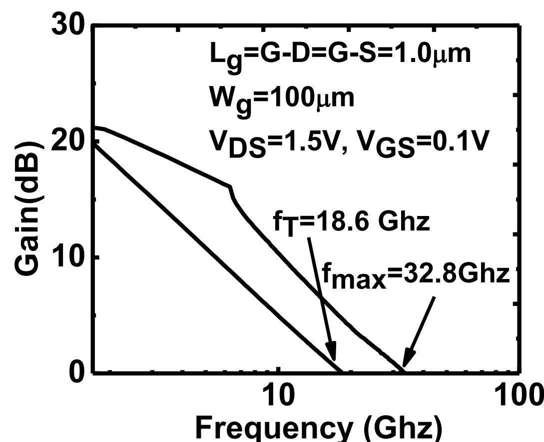

Fig.6. RF characteristics of 1-µm MOS-HEMT on Si

We attribute the good DC and RF performance to the following three main aspects. The first factor is the high-quality epitaxial layers grown on Si substrate by MOCVD [15], as evidented by the high electron mobility and low sheet resistance from Hall measurement. The second factor is the unpinned Fermi level realized by ALD, which could be observed from the X-Ray photoelectron spectroscopy (XPS) analysis shown in Fig.7 and capacitance-voltage (C-V) response shown in Fig.8. Fig.7 illustrates the As-*3d* and As-*2p* XPS spectra for InGaAs surface before and after the ALD process. The AsO_x nearly vanishes due to the self-cleaning effect of the ALD [16]. The lack of high-quality, thermodynamically stable gate dielectric on GaAs or III-V materials remains the main obstacle to realize III-V MOSFET. The understanding of the interface physics and chemistry of the III-V's is still quite limited, though enormous research efforts have been invested in this field. A consensus has

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been emerged that a significant amount of As_2O_3, As_2O_5 and elemental As present in native oxides pin the Fermi

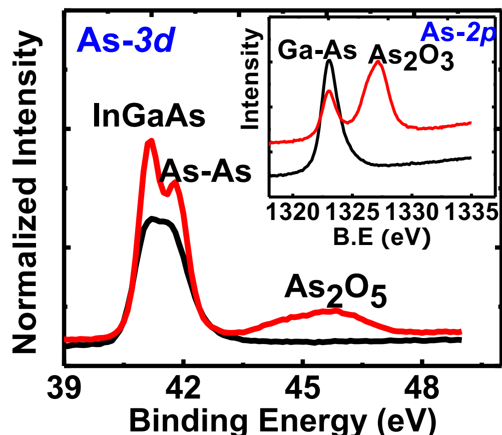

Fig.7. As-*3d* and As-*2p* XPS spectra for InGaAs surface. **Red line:** XPS of InGaAs surface just after HCl pretreatment but without ALD process. **Black line**: InGaAs and Al_2O_3 interface after ALD process.

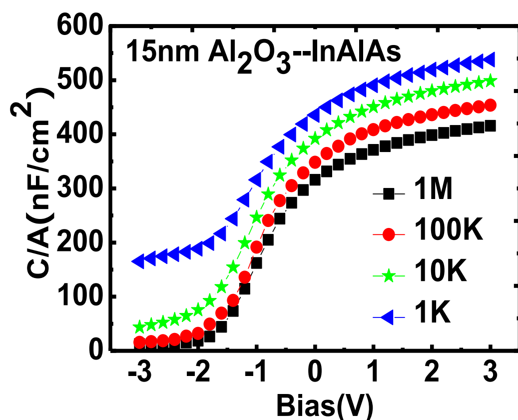

Fig.8. Multi-frequency CV curve for Al_2O_3-InAlAs capacitor measured at several frequencies

level of GaAs and they are not favorable for an ideal gate dielectric [17]. Fig.8 exhibits the multi-frequency C-V response of the MOS-HEMT on Si, which further indicates that the Fermi Level is unpinned. However, a large frequency dispersion in the accumulation region was observed from the CV curve, which shows that the interface quality still needs further optimization. The third factor is the low-temperature process which achieves low contact resistance without degrading the interface between oxide and III-V materials.

4. Conclusion

We have demonstrated $In_{0.53}Ga_{0.47}As/In_{0.51}Al_{0.49}As$ MOS-HEMTs grown on Si substrates by MOCVD for the first time. A maximum drain current of 415 mA/mm and extrinsic transconductance of 329 mS/mm were achieved. The preliminary DC and RF results show the potential of III-V MOSFETs built on Si substrates for future high-speed and low-power logic applications. On the other hand, to further improve the device performance, the interface quality and the device structures still need further optimization.

5. Acknowledgement

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6. References

[1] Y. Xuan, Y .Q. Wu, and P. D. Ye, “High-performance Inverstion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm” *IEEE Electron Device Lett.*, vol.29,no.4, pp 294-296, 2008

[2] Y.Q.Wu, M. Xu, R. S. Wang, O. Koybasi and P.D. Ye, “High Performance Deep-Submicron Inversion-Mode InGaAs MOSFETs with maximum Gm exceeding 1.1 mS/um: New HBr Pretreatment and Channel Engineering” *IEDM Tech. Dig.*, pp.323-326, 2009

[3] I. Thayne, X. Li, W. Jansen *et al.*, “Development of III-V MOSFET Process Modules Compatible with Silicon ULSI Manufacture,” *Electrochem. Soc. Transaction,* vol.25, no.7, pp.385-389. 2009.

[4] R. J. W. Hill, D. A. Moran, X. Li, *et al.,* “ Enhancement-Mode GaAs MOSFETs with an $In_{0.3}Ga_{0.7}As$ channel, a mobility of over 5000 $cm^2/V \cdot s$, and transconductance of over 475 $\mu S/\mu m$, ” *IEEE Electron Device Lett.,* vol.28,no.12, pp. *1080-1082,2007*

[5] M. Passlack, K. Rajagopalan, J. Abrokwah, R. Droopad, “Implant-Free High-Mobility Flatband MOSFET: Principles of Operation” *IEEE Electron Device Lett.,* vol.53, no.12, pp. *2454-2456, 2006*

[6] U. Singisetti, M. A. Wistey, G. J. Burek *et al.,* “InGaAs channel MOSFET with self-aligned source/drain MBE regrowth technology” *Proc 20th Intern.Conf. on IPRM* (2008), pp.1-6, 2008

[7] M. Radosavljevic, B. C. Kung, S. Corcoran *et al.*, “advanced high-K gate dielectric for high-performance short-channel InGaAs quantum well field effect transistors on Si substrate for low power logic applications” in *IEDM Tech. Dig.*, pp.319-322, 2009

[8] T. D. Lin, H. C. Chiu, P. Chang *et al*, “High-performance self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistor with Al_2O_3 /$Ga_2O_3(Gd_2O_3)$ as g ate dielectrics,” *Appl. Phys. Lett.* 93, 033516, 2008

[9] M. K. Hudait, G. Dewey, S. Datta *et al*., "Heterogeneous integration of enhancement mode $In_{0.7}Ga_{0.3}As$ quantum well transistor on silicon substrate using thin (< 2um) composite buffer architecture for high-speed and low-voltage (0.5V) logic applications," *IEDM Tech. Dig.*, pp.625, 2007

[10] H. Becke, R. Hall and J.White, "Gallium arsenide MOS transistors," *Solid State Electron.,* vol. 8, no. 10, pp. 813–823, 1965.

[11] F. Ren, J. M. Kuo, M. Hong *et al*., "Ga_2O_3 (Gd_2O_3) /InGaAs Enhancement-Mode n-Channel MOSFET's" *IEEE Electron Device Lett.* vol.19,no.8*,* pp. *309-311,2007*.

[12] Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye, "High Performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2, and HfAlO as gate dielectrics" *IEDM Tech. Dig.*, pp.637-640, 2007

[13] D. I. Garcia, D. Shahrjerdi, V. Kaushik, and S. K. Banerjee, "Physical and electrical characterizations of metal-oxide-semiconductor capacitors fabricated on GaAs substrates with different surface chemical treatments and Al_2O_3 gate dielectric" *J. Vac. Sci. Technol. B,* vol.27, no.6, pp.2390-2394, 2009.

[14] N. Li, E. S. Harmon, J. Hyland *et al*., "Properties of InAs Metal-Oxide Semiconductor structures with Atomic-Layer-deposited Al_2O_3 dielectric" *Appl. Phys. Lett.* 92, 143507, 2008.

[15] K. M. Lau, C. W. Tang, H. O. Li and Z. Y. Zhong, "AlInAs/GaInAs mHEMTs on Silicon Substrates Grown By MOCVD" in *IEDM Tech. Dig.,* pp.723-724, 2008.

[16] C. W. Cheng, J. Hennessy, D. Antoniadis, and E. A. Fitzgerald, "Self-cleaning and surface recovery with arsine pretreatment in ex situ atomic-layer-deposition of Al2O3 on GaAs" *Appl. Phys. Lett.* 95, 082106, 2008.

[17] S. Oktyabrsky and P. D. Ye *et al.*, "Fundamentals of IIIV Semiconductor MOSFETs," Springer, 1st edition, Chapter 7, pp 174, 2010.

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