High-performance implant-free InGaAs MOSFETs on GaAs substrate grown by MOCVD

Xiuju ZHOU, Chak Wah TANG, Haiou LI, Peng CHEN, and Kei May LAU
Department of Electronic and Computer Engineering,
Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

Abstract

High-performance implant-free $In_{0.53}Ga_{0.47}As$-channel MOSFETs grown on GaAs substrates by Metalorganic Chemical Vapor Deposition (MOCVD) are demonstrated. Atomic-layer-deposited (ALD) Al_2O_3 was used as gate dielectric on top of a δ-doped $In_{0.53}Ga_{0.47}As/In_{0.51}Al_{0.49}As$ metamorphic heterojunction structures grown on GaAs substrates. A 1-μm gate-length MOSFET with 15nm Al_2O_3 shows a maximum drain current of 590 mA/mm and peak Gm of 501 mS/mm. To the best of our knowledge, these are the highest reported values to date for III-V MOSFETs on GaAs substrates. The maximum gate leakage is 7.2nA/mm at the forward gate bias of 4V and the on resistance is 1491 Ω·μm

1. Introduction

As the scaling of Si-based CMOS is reaching its fundamental physical limits in the next decade, III-V compound semiconductors are considered as promising channel materials due to their superior electron transport properties. For the past four decades, there have been great efforts in seeking high-quality and thermodynamically stable gate dielectrics for III-V MOSFETs[1-6]. Specifically, InGaAs channel MOSFETs on InP substrates have been intensively investigated by a few groups [7-10]. However, in addition to the high cost and brittleness, the supply of InP large area substrates are limited. It is more desirable to use commercially available large area GaAs, even during the technology development stage, making them one step closer to the eventual goal of large scale integration.

Moreover, it is well known that III-V-based MOSFETs usually have relatively low thermal tolerance in the device fabrication process. For instance, the interface between the gate oxide and III-V materials can be easily degraded during high-temperature processes such as the annealing step after ion-implantation in conventional inversion-mode MOSFETs. In this work, no thermal annealing is needed in the entire fabrication process. High-performance implant-free $In_{0.53}Ga_{0.47}As$ MOSFETs on GaAs substrates grown by MOCVD have been demonstrated. The maximum drain current Idss and peak transconductance are 590mA/mm and 501mS/mm, respectively, which are the record-high values for 1-μm gate-length III-V MOSFET on GaAs substrates[11-12].

2. Experiment

Figure 1 shows a schematic cross-section of the device structure. The metamorphic $In_{0.53}Ga_{0.47}As/In_{0.51}Al_{0.49}As$ heterojunction epitaxial layers lattice-matched to InP were grown on 4-inch semi-insulating GaAs substrates by MOCVD[13]. The detailed epitaxial structure is shown in Table.1.

For device fabrication, Firstly, mesa isolation was formed by wet chemical etching down to the low-temperature grown InAlAs buffer after surface cleaning. Then Succinic Acid/hydrogen peroxide with high selectivity of InGaAs/InAlAs was used to realize the gate recess. 15nm Al_2O_3 was deposited by Atomic Layer Deposition(ALD) at 300˚C immediately after

978-1-4244-5798-4/10/$26.00 ©2010 IEEE

surface pretreatment in 10% HCl for 3min. Afterward, Al_2O_3 in the source/drain regions was removed by Buffered-Oxide-Etch, non-alloy ohmic contacts were obtained by electron-beam evaporation of a six-layer metal system of Ni/Ge/Au/Ge/Ni/Au and lift off. Finally the gate was made by evaporation of Ti/Pt/Au and lift off. There is no annealing in the entire fabrication process.

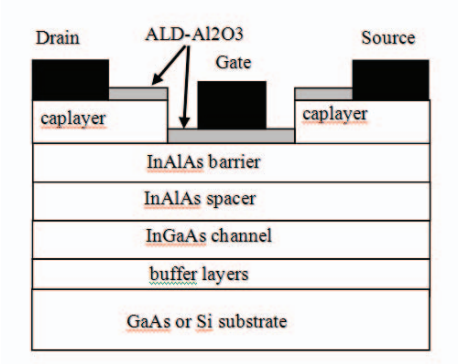

Figure.1. schematic cross section of InGaAs MOSFETs

Table 1. epitaxial layers structure of InGaAs MOSFET

$In_{0.53}Ga_{0.47}As$: Si, 5×10^{18} cm^{-3}, 15nm	Cap layer
Undope $In_{0.51}Al_{0.49}As$, 25nm	Barrier
Si δ-doping, 4×10^{12} cm^{-2}	Delta doping
Undoped $In_{0.51}Al_{0.49}As$, 5nm	Spacer
Undoped $In_{0.53}Ga_{0.47}As$, 18nm	Channel
Undoped HT- $In_{0.51}Al_{0.49}As$, 100nm	Buffer 6
Undoped LT- $In_{0.51}Al_{0.49}As$, 200nm	Buffer 5
Undoped LT-InP, 100nm	Buffer 4
Undoped HT-InP, 650nm	Buffer 3
Undoped LT-InP, 110nm	Buffer 2
Undoped HT-GaAs, 100nm	Buffer 1
Semi-insulating GaAs Substrate	

.

3. Results and Discussion

Figure 2 shows the transistor characteristics of an InGaAs MOSFET with a gate bias from -1 to 1.4 V in steps of +0.4V. For a typical 1um-gate length device, the maximum drain current (Idss) measured was 590mA/mm at Vgs=1.4 V and Vds=2 V. Figure 3 shows the transfer characteristics at a drain bias of 1.5V. A peak transconductance (Gm_{max}) of 501mS/mm was achieved at Vgs=0.3V. The on resistance was calculated to be 1491 Ω·μm from the Ids-Vds cruve. The gate leakage current characteristic of the MOSFETs on GaAs is shown in Figure 4. The maximum gate leakage was 7.2 nA/mm at a forward gate bias of 4V. Without any ohmic contact annealing, a low contact resistance of 0.46Ω-mm and sheet resistance of 84Ω/sq was achieved from transmission line measurements (TLM).

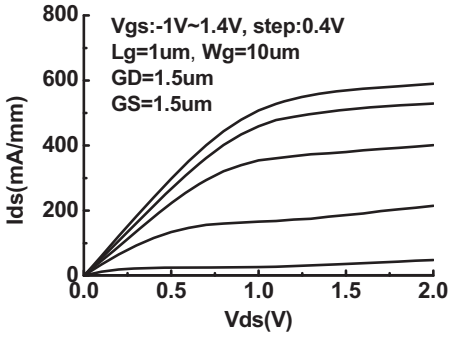

Figure2. *I-V* characteristics of InGaAs MOSFET

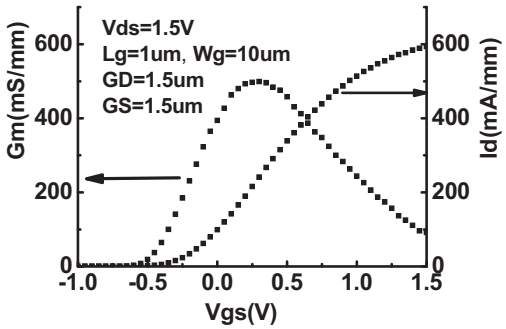

Figure3. transfer characteristics of InGaAs MOSFET

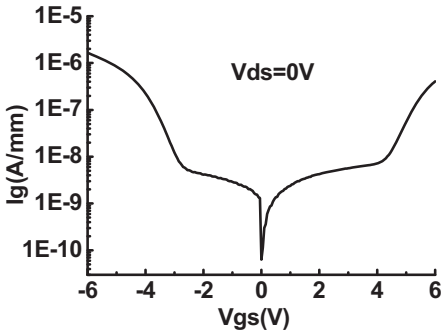

Figure 4. Gate leakage current of InGaAs MOSFET

From our data, we observed an obvious improvement for DC characteristics including Idss and Gm for implant-free $In_{0.53}Ga_{0.47}As$ MOSFETs on GaAs

substrates, compared to previously published results [12]. We ascribe this improvement to the following three major factors. First, the low ohmic contact resistance achieved by optimized contact metallization and the highly-doped InGaAs cap-layer. Second, a high-quality epitaxial InGaAs/InAlAs heterostructure with high mobility and low sheet resistance. Third, There is no thermal process involved in our entire fabrication. It is well known that III-V materials have a low thermal budget and it is better to avoid high temperature processes (>300˚C). Especially in InGaAs MOSFET, degradation of the interface between gate oxide and the III-V materials after high-temperature process such as ion-implantation activation in inversion-mode MOSFET has been observed. Moreover, the optimized ALD process also achieved a high-quality Al_2O_3 and a good interface between oxide/InGaAs without post deposition annealing.

4. Summary

We have demonstrated high-performance implant-free $In_{0.53}Ga_{0.47}As$ MOSFETs grown on GaAs substrates by MOCVD. Without any thermal annealing in the entire process, 1-μm gate-length devices show a maximum Idss of 590mA/mm and transconductance of 501mS/mm, which are the highest reported values to date for III-V MOSFETs on GaAs substrates. These DC results suggest great potential of III-V MOSFETs for future high-speed and low-power logic applications [14].

Acknowledge

The authors would like to thank Z.Y.Zhong, Q.Li, M.Li, Q.Luo, H.Liang, Z.J.Liu and T.D.Huang for the valuable discussions. The support of the Nanoelectronics Fabrication Facility (NFF), in particular by H.Li is acknowledged.

Reference

[1] H. Becke, R. Hall, and J. White, *Solid State Electron.*, 8, p.813–823 (1965).

[2] M. Hong, J.P. Mannaerts and J.E. Bower et al., *J. Crystal Growth,* 175/176, p.422-424 (1997)

[3] F. Ren, M. Hong, W. S. Hobson, *solid-state electronics*, 41, p.1751-1753(1997)

[4] Y.Xuan, Y.Q.Wu et al. *IEDM Tech. Dig.* 637(2007)

[5] InJo Ok, H. Kim et al., *IEDM Tech. Dig.* 829 (2006)

[6] H C. Lin，T. Yang and H. Sharifi, Appl. Phys. Lett, 91, p.212101 (2007)

[7] Y.Xuan, T.Shen et al., *IEDM Tech. Dig.* 371(2008)

[8] R.J.W.Hill, R.Droopad, D.A.J.Moranet et al., *Electronics Letters*, 44 (2008).

[9] T.D.Lin, H.C.Chiu, P.Chang et al., *Applied Physics Letters* 93, p.033516(2008)

[10] U.Singisetti, M.A.Wistey, G.J.Burek et al., *IEEE Electron Device Lett.* 30, p.1128(2009)

[11] M. Passlack, R. Droopad, et al., CS MANTECH Conference, p.235(2007)

[12] R.J.W.Hill, D.A.J.Moran, X.Li et al., *IEEE Electron Device Lett.* 28, p.1080(2007)

[13] K.M. Lau, C.W.Tang, H.O.Li et al., *IEDM Tech. Dig.* 723(2008)

[14] R.Chau, B.Doyle, S.Datta et al,. *Nature Materials*, 6, 810-812(2007)