ECS Transactions, 28 (5) 227-231 (2010)
10.1149/1.3367954 ©The Electrochemical Society

Hetero-epitaxy of III-V Compounds by MOCVD on Silicon Substrates

Chak Wah TANG, Zhenyu ZHONG, and Kei May LAU

Department of Electronic and Computer Engineering
Hong Kong University of Science and Technology
Clear Water Bay, Kowloon, Hong Kong

Over the past few years, we have successfully developed hetero-epitaxial techniques to grow device quality III-V and III-nitride structures on silicon substrates by MOCVD. We have demonstrated very good device performance with conventional III-V HEMT (High Electron Mobility Transistor) structures grown and fabricated on Si substrates. These devices were nearly lattice-matched to InP. Unlike previous approaches of using a Ge buffer, compositional grading, or superlattices, we adopted similar techniques that have been well developed for hetero-epitaxy of III-nitrides on sapphire substrates. A well-tuned nucleation layer deposited at low-temperature followed by regular high-temperature epitaxy is effective in producing good quality layers for device applications. Aided by in-situ photoreflectance anisotropy and other material characterization tools, device quality epi-layers can be grown and very good transistor characteristics were measured.

Introduction

After decades of separate development for different applications, silicon and III-V compounds are now considered by various semiconductor communities that merging of their technologies would bring new and advanced functionalities and capabilities. Si based devices and circuits have been primarily advanced for logic, signal processing, and memory applications while III-V semiconductor devices are traditionally for photonics such as lasers, modulators, LEDs, and microwave/RF applications. In recent years, interests in III-V (including III-nitrides) devices for high speed logics and power switching are mounting. Meanwhile, silicon photonics has taken on a life of its own and developed into a vibrant field of research, taking advantage of the well-developed Si technologies for optical interconnects, signal processing, routing, and switching. Many exciting research programs are being carried out in academic and industrial laboratories in these areas. However, many commercial PICs (photonic integrated circuits) are still being fabricated with InP substrates.

Ideally, integrating all the components on a Si platform utilizing the most advanced silicon manufacturing technologies is the future dream of all the research communities involved. It is well known that III-V transistors can operate up to three times faster with 10X lower power consumption than Si NMOS with the same device dimensions. However, integration with Si is the key to successful deployment of this technology.

Direct epitaxial growth of GaAs (InP and other alloys) on Si was a favorite research topic in the 1980s and was essentially ‘abandoned’ for various reasons. A majority of the work was aimed for OEIC (Optoelectronic Integrated Circuits) applications. Recent revitalized interest, with the push from the silicon industry, has placed the focus on CMOS compatible configurations and technologies. With the huge

mismatch in lattice constants and structure, thermal expansion coefficients, the quality of the III-V layers grown on Si are largely compromised compared with those on lattice-matched substrates. Various techniques can be used to accommodate these differences and it is essential to determine different material requirements for various applications.

Material growth and characterization

$Ga_{0.47}In_{0.53}As$ quantum well (QW) channel HEMT device layers nearly lattice-matched to InP were grown on silicon substrates using an Aixtron AIX-200/4 MOCVD system with EpiRAS-2000 installed for reflectance anisotropic (RA) measurements. All the substrates used were standard 4-inch exact-(100) n- or p-type Si. A two step growth technique was utilized in this experiment. TMGa, TMIn, AsH_3 and PH_3 were used as gallium, indium, arsenic and phosphorus precursors. Prior to growth, the silicon wafer was cleaned and de-oxidized by H_2SO_4:H_2O_2 and diluted HF, respectively. After loading into the reactor, the substrate was heated up to 850°C for thermal cleaning. It was cooled down to 425°C for the GaAs nucleation layer growth. During the substrate temperature cooling from 850°C to 600°C, with reactor pressure equal to 100mbar, arsine in an H_2 ambient was flowed into the reactor. The initial nucleation process is very important for GaAs on silicon since silicon is a non-polar material which is different from polar GaAs. It is reported that flowing Arsine above 750°C could help forming double monolayer steps on Silicon surface as well as a stable As prelayer, which can prevent APD formation (1). The growth temperature of the composite buffer layers varied from 425°C to 670°C. The active layers were grown at a substrate temperature equal to 670°C.

The detailed epitaxial structure design including the composite buffer is shown in Table 1 (2). The total thickness of the composite buffer was about 1.6 μm.

Layer function	**Material**	**Doping**	**Thickness**
Cap/contact layer	$Ga_{0.47}In_{0.53}As$	Si, 5×10^{18} cm^{-3}	15 nm
Barrier	$Al_{0.50}In_{0.50}As$	Undoped	30 nm
Si δ-doping	Si	$4 – 8 \times 10^{12}$ cm^{-2}	undetermined
Spacer	$Al_{0.50}In_{0.50}As$	Undoped	5 nm
Channel	$Ga_{0.47}In_{0.53}As$	Undoped	32 nm
Buffer 5	HT- $Al_{0.50}In_{0.50}As$	Undoped	120 nm
Buffer 4	LT- $Al_{0.47}In_{0.53}As$	Undoped	180 nm
Buffer 3	HT-InP	Undoped	730 nm
Buffer 2	LT-InP	Undoped	150 nm
Buffer 1	HT-GaAs	Undoped	450 nm
Nucleation	LT-GaAs	Undoped	10 nm
Substrate	Silicon (100)	n-type	300 μm

Table 1 Layered structure of mHEMT on Si substrate

The growth process was monitored using the color plot mode in an EpiRAS *in-situ* monitoring system (3), detection is being made at two wavelengths: 1.6eV and 2.55eV. As absorption of GaAs or InP based materials are significantly different at these wavelengths (low absorption at 1.6eV, strong absorption at 2.55eV), the shape of the Fabry-Perot-oscillations are considerably different. The high energy measurement (2.55eV) is also much more sensitive to the surface morphology and roughness. Shown

in Figure 1 are the RAS scans during the growth of the complete structure at these two wavelengths.

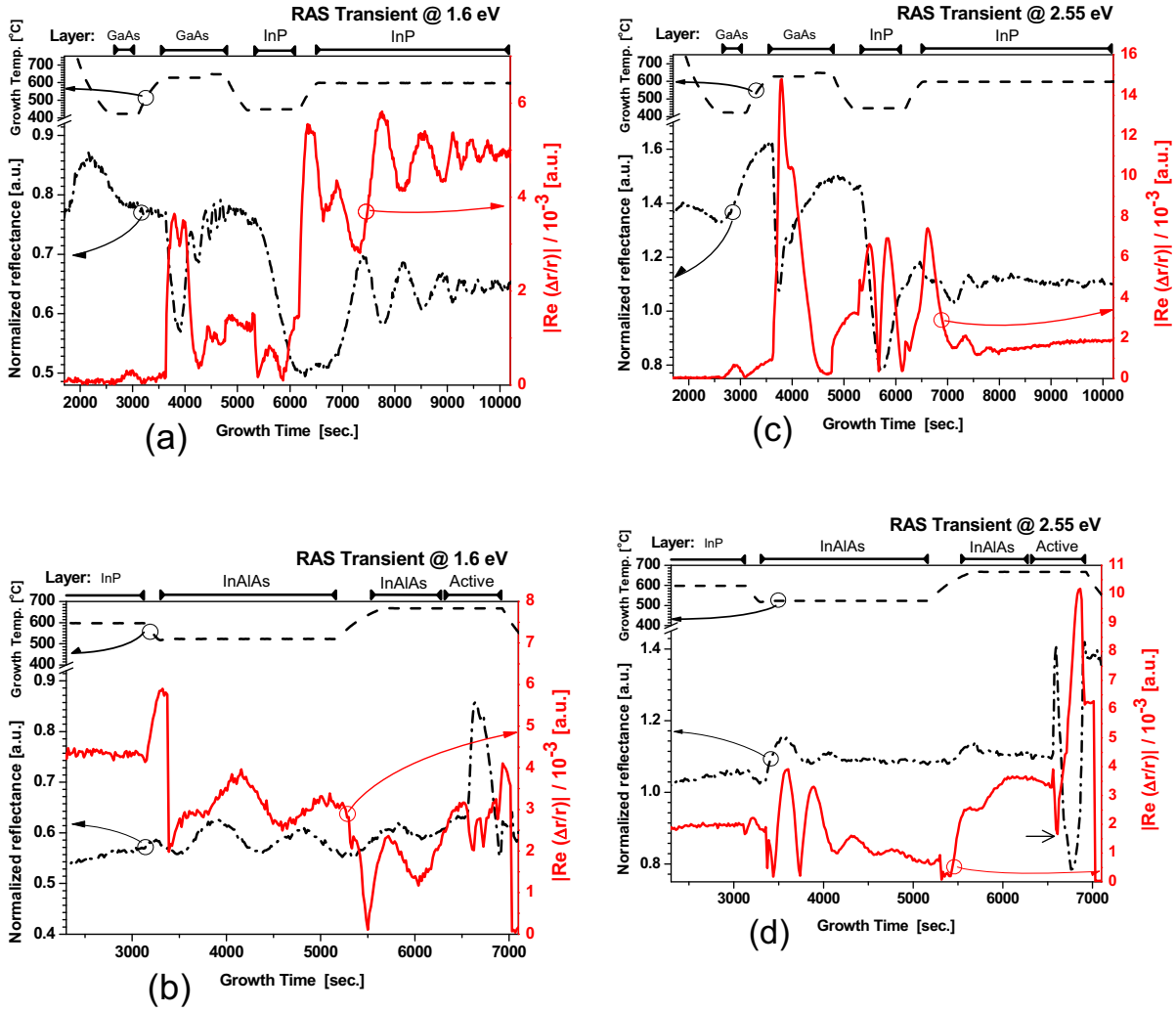

Figure 1. RAS transients measured simultaneously as the reflectance transients for a complete device structure grown on a silicon substrate. (a) and (b) show a set of transients at 1.6eV. (c) and (d) show a set of transients at 2.55eV.

The grown HEMT structure was characterized by 4-crystal high-resolution X-Ray Diffraction to evaluate the layered structure. Philip's X'Pert Epitaxy simulator was used for the curve fitting to identify the compositions of the alloys. In Fig. 2. Peak a, b, c, d represent the epitaxial layers grown on the Si substrate corresponding to GaAs, LT-$Al_{0.52}In_{0.48}As$, InP, and HT-$Al_{0.44}In_{0.56}As$, respectively. There are some slight mis-matches to our original designed structures as in shown in Table 1. All peaks are clearly resolved and sharp. This is different from MBE growth designs which involve graded composition control in the buffer. To match the measured and fitted peak positions, it shows that peaks a and c have relaxation of +102% and +101% respectively, indicating the residual tensile stress caused by thermal mismatch. The indium composition of peaks b and d are around 50% and 56%, respectively.

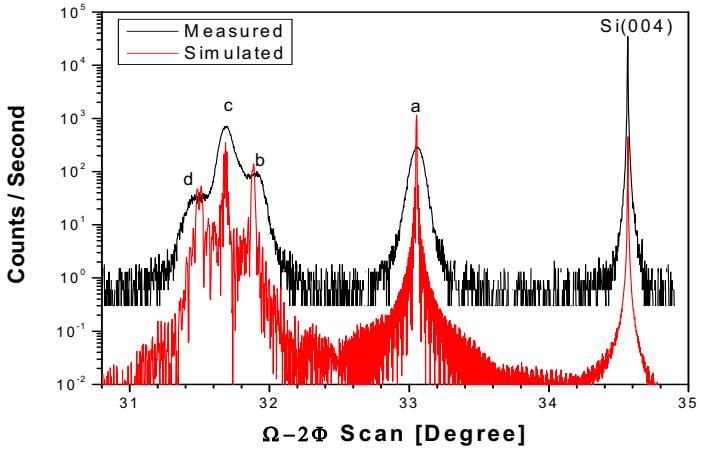

Fig. 2 Material and composition characterization by High resolution X-Ray Diffraction.

Hall mobility measurements using the van der Pauw method were carried out at 300K and 77K, to evaluate the quality of the 2-DEG, usually indicated by the amount of mobility enhancement at 77K from room temperature. The electron mobilities of the mHEMT structure, with the best device results, were 4540 and 14,000 cm^2/V-s with sheet carrier densities of 8×10^{12} cm^{-2} and 5×10^{12} cm^{-2} at 300K and 77K, respectively.

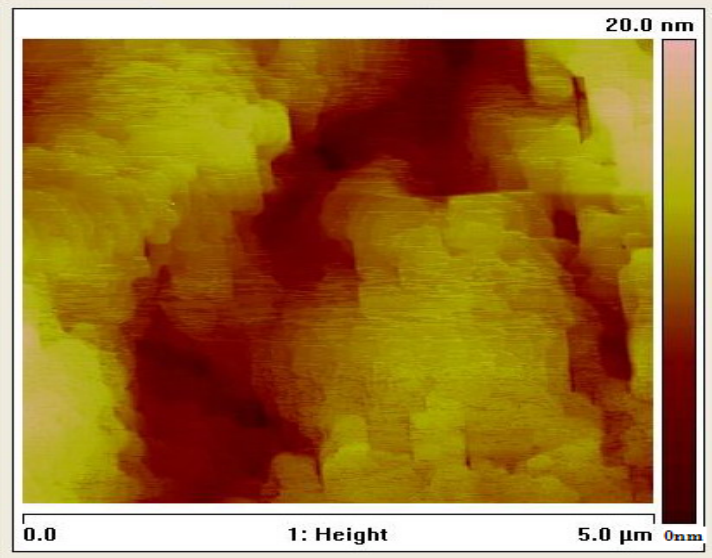

Fig. 3 AFM image of 5× 5µm^2 scan of a mHEMT structure grown on Si substrate.

Fig. 3 shows an AFM image of the typical mHEMT structure. The Root Mean Square (RMS) value of surface roughness is 3 nm across a scan area of 5×5µm^2, which is somewhat rougher than that of similar structure grown on GaAs substrate (4). Large islands can be observed from the AFM micrograph, which is different from the surface morphology obtained by other groups, where elongated islands are presented. The difference is due to the different relaxation mechanism: the mismatch is accommodated by low temperature nucleation buffer in our case while graded AlInAs buffer help releasing the stress gradually (2).

Device Results and characteristics

Depletion-mode $Al_{0.50}In_{0.50}As/Ga_{0.47}In_{0.53}As$ mHEMTs grown on n-type Si substrates were fabricated. The device gate length was 1.0-μm and the spacing between gate-source and gate-drain were both 1.5-μm. Gate recess was formed using a citric acid-based etchant to remove the highly-doped GaInAs cap layer. Ti/Pt/Au was used as the Schottky gate contact. No passivation was used on the devices. The maximum drain current measured at V_{GS}=0.4V and V_{DS}=1.5V was 760mA/mm, while the maximum extrinsic transconductance achieved was 613mS/mm at V_{GS}= -0.5V and V_{DS}=1.5V. The device is a depletion-mode transistor with a threshold voltage V_{th} of around -1.0V. On-wafer S-parameters measurements were carried out on 1.0 × 100μm^2 mHEMTs using Cascade Microtech probes with an HP8722 network analyzer from 0.1 to 39.1GHz. Open on-wafer de-embedding structures were used to determine the parasitic capacitances of the probe pads and to de-embed the short circuit current gain $|h_{21}|$. The current gain cut-off frequency (f_T) was determined to be 36.9GHz. Extrapolating the de-embedded data from 39.1GHz at -20dB/decade resulted in an f_{max} of 55.6GHz. The optimum bias condition for maximum unity current gain cut-off frequency was at V_{GS}=-0.4V and V_{DS}=1.5V for this device.

Acknowledgments

This work was supported by a CERG grant (615207) from the Research Grants Council of Hong Kong and Intel Corporation.

References

1. S.F. Fang, K. Adomi, S. Lyer, H. Morkoc, H. Zabel, C. Choi and N. Otsuka,, *J. Appl. Phys.*, 68, R-31 (1990).
2. K.M. Lau, C.W. Tang, H.O. Li, and Z.Y. Zhong, *IEDM Tech Diges.*, p.723, (2008).
3. http://www.laytec.de/compounds-applicationnotes.html
4. H. O. Li, C. W. Tang, K. J. Chen, and K. M. Lau," *IEEE Electron Device Lett.*, 29, p.561 (2008).