0.3-µm Gate-length Metamorphic AlInAs/GaInAs HEMTs on Silicon Substrates by MOCVD

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Abstract

Fabrication and performance of high-frequency 0.3-µm gate-length depletion-mode metamorphic $Al_{0.50}In_{0.50}As$/ $Ga_{0.47}In_{0.53}As$ high electron mobility transistors (mHEMT) grown by Metalorganic Chemical Vapor Deposition (MOCVD) on n-type silicon substrates is reported. Using a combined optical and e-beam photolithography technology, submicron mHEMT devices on Si have been achieved. A maximum trans-conductance up to 739mS/mm was measured. The unity current gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) were 72.4 and 77.3GHz, respectively. An input capacitance to gate-drain feedback capacitance ratio, Cgs/Cgd, of 6.8 and a voltage gain, g_m/go, of 6.9 are observed in the device.

1. Introduction

In recent years, there has been a revitalized interest in growing III-V epitaxial layers on Si substrates, by molecular -beam epitaxy (MBE) and MOCVD. Unlike past efforts focusing on optoelectronic applications two decades ago, recent emphases are for applications in high speed, and low power circuits. Silicon is the most mature and widely used in the IC industry, and will continue to progress in its manufacturing technologies in the foreseeable future. High-speed silicon-based devices and circuits have been advancing following the infamous Moore's Law for decades, primarily through shrinkage of the device dimensions. Meanwhile, III-V semiconductor devices, such as AlInAs/GaInAs two-dimensional electron gas (2-DEG) systems, have been shown to operate with reduced DC power dissipation for the same speed performance, or higher gain in speed performance for the same power compared to conventional silicon devices [1-5]. To combine the advantages of both materials, the most promising solution is to integrate compound semiconductor devices with silicon technologies. With such a motivation and significant advances in epitaxial technologies from the 1980s, direct growth of good quality III-V materials on silicon substrates for device applications is imminent. There are many technological challenges to be overcome due to the large density of threading dislocation defects in the epi-layers resulting from the lattice mismatch and difference in thermal expansion coefficient between the Si substrate and grown layers [6]. Although MBE has been the more advanced technology in III-V electronic device development, MOCVD is deemed more compatible with traditional Si manufacturing technologies and has been used for manufacturing of III-V optical devices and HBTs. Furthermore, it has been demonstrated recently that metamorphic device structures such as InP/GaAsSb/InP mHBTs or AlInAs/GaInAs mHEMTs can be grown on GaAs substrates by MOCVD [7-9]. Among them, AlInAs/GaInAs HEMTs lattice-matched to InP have the best frequency and low-noise performance. If good quality GaAs can be deposited on Si substrates, it would be a logical step to combine with the metamorphic device technologies for integration of high speed HEMTs on silicon.

In this paper, we describe the growth and fabrication of submicron AlInAs/GaInAs mHEMTs grown on silicon substrates by MOCVD. Unlike previous techniques such as the use of a Ge intermediate layer or composition grading buffers, a unique composite buffer with a relative small thickness for the transition from Si to the active device layers was developed. 0.3-µm gate-length devices were fabricated and comprehensive DC and RF device characteristics are reported.

2. Materials growth and device fabrication

$Ga_{0.47}In_{0.53}As$ quantum well (QW) channel HEMT device layers lattice-matched to InP were grown on silicon substrates using an Aixtron AIX-200/4 MOCVD system. Standard 4-inch exact- (100) oriented n-type Si substrates were used. The detailed epitaxial structure design including the composite buffer is shown in Figure.1. The total thickness of the composite buffer is about 1.6 µm, which is smaller than the previous report [2].

The Hall mobility were 6180 and 16,500 cm^2/V-s with sheet carrier densities of 8×10^{12} cm^{-2} and 5×10^{12} cm^{-2} at 300K and 77K, respectively. Figure.2 shows an AFM image of the typical mHEMT structure. The Root Mean Square (RMS) value of surface roughness is 3.1nm across a scan area of $5 \times 5 \mu m^2$, which is somewhat rougher than that of similar structure grown on GaAs substrate [9].

Depletion-mode $Al_{0.50}In_{0.50}As/Ga_{0.47}In_{0.53}As$ mHEMTs grown on n-type Si substrates were fabricated. The device gate length was 0.3-µm and the spacing between gate-source and gate-drain were both 1.0-µm. Firstly, mesa isolation was formed by wet chemical etching down to the low-temperature (LT) grown AlInAs buffer. A six-layer metal system (Ni/Ge/Au/Ge/Ni/Au) was evaporated to form source/drain ohmic contacts. The non-alloyed ohmic contact resistance Rc was determined to be 0.065 Ω-mm by

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$Ga_{0.47}In_{0.53}As$: Si, 5 × 10^{18} cm^{-3}, 15nm	Cap layer
Undoped $Al_{0.50}In_{0.50}As$, 30nm	Barrier
Si δ-doping, (4-8) × 10^{12} cm^{-2}	Delta doping
Undoped $Al_{0.50}In_{0.50}As$, 5nm	Spacer
Undoped $Ga_{0.47}In_{0.53}As$, 32nm	Channel
Undoped HT- $Al_{0.50}In_{0.50}As$, 120nm	Buffer 5
Undoped LT- $Al_{0.47}In_{0.53}As$, 180nm	Buffer 4
Undoped HT-InP, 730nm	Buffer 3
Undoped LT-InP, 150nm	Buffer 2
Undoped HT-GaAs, 450nm	Buffer 1
Undoped LT-GaAs, 10nm	Nucleation
n-type Silicon (100) Substrate	

Figure.1 Nominal layered structure of mHEMT device.

TLM method. 0.3-μm T-gate was fabricated using two-stage photolithography technology, which is the mixture technology with optical and e-beam photolithography. First, a 100nm-thick SiN_x film was deposited by PECVD; and the gate footprint pattern was formed by e-beam photolithography. After etching of the SiN_x film to obtain gate footprint pattern by reactive ion etching (RIE), the gate-head pattern was formed by optical photolithography process. Gate recess was formed using a SA-based etchant to remove the highly-doped GaInAs cap layer. Finally, Ti/Pt/Au was deposited as the Schottky gate contact. No passivation was used on the devices.

3. DC characteristics

Device output and transfer characteristics of 0.3-μm-gate-length mHEMTs were obtained. The DC current-voltage characteristics of a typical AlInAs/GaInAs mHEMT are shown in Figure.3. The maximum drain current measured at V_{GS}=0V and V_{DS}=1.0V was 900mA/mm. The device has a maximum extrinsic trans-conductance of 739mS/mm shown in Figure.4, and a g_o of 107mS/mm. The voltage gain, g_m/go, is 6.9. The output conductance is a little large, which can improve by optimizing the device structure, such as a larger gate-drain gap L_{gd}. The device is a depletion-mode transistor with a threshold voltage V_{th} of around -1.4V. The gate leakage current characteristics of the mHEMT were shown in the inset of Figure.4. The reverse gate leakage may seem slightly high because no passivation or plasma treatment was administered.

4. RF performance

On-wafer S-parameters measurements were carried out on 0.3×100μm^2 mHEMTs using Cascade Microtech probes and an HP8722 network analyzer from 0.1 to 39.1GHz. Open on-wafer de-embedding structures were used to determine the parasitic capacitances of the probe pads and to de-embed the short circuit current gain $|h_{21}|$.

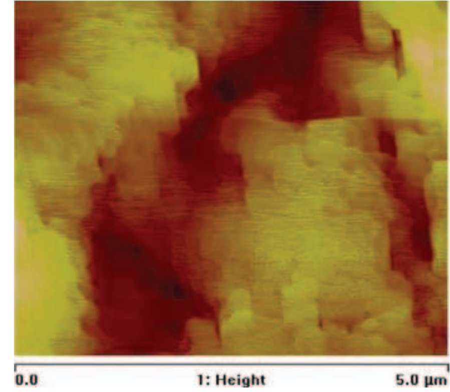

Figure.2 AFM image of a typical Si-based mHEMT structure.

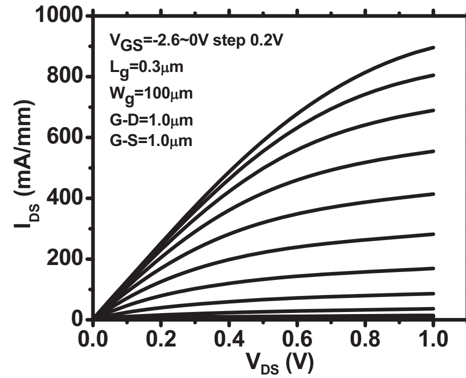

Figure.3 DC *I-V* characteristics of a 0.3×100μm^2 mHEMT.

Figure.5 shows the current gain and MSG/MAG as a function of frequency for 0.3×100μm^2 mHEMTs. The current gain cut-off frequency (f_T) was 72.4GHz. Extrapolating the de-embedded data from 39.1GHz at -20dB/decade resulted in f_{max} of 77.3GHz. The optimum bias condition for maximum unity current gain cut-off frequency was determined to be V_{GS}=-0.9V and V_{DS}=1.0V. An input capacitance to gate-drain feedback capacitance ratio, Cgs/Cgd, is 6.8, which was determined by equivalent circuit modeling of measured 5-25GHz S-parameters. Figure.6 shows the dependence of f_T and f_{max} of Si-mHEMT on gate-source bias voltage measured at V_{DS}=1.0V.

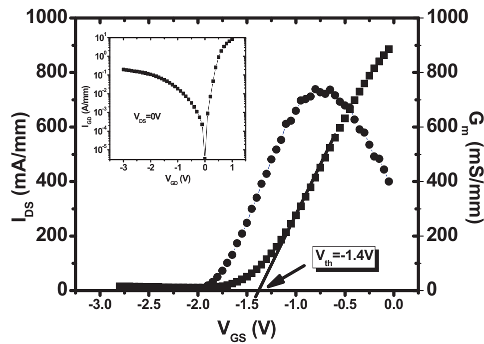

Figure.4 Transfer characteristics of 0.3×100 μm^2 mHEMT.

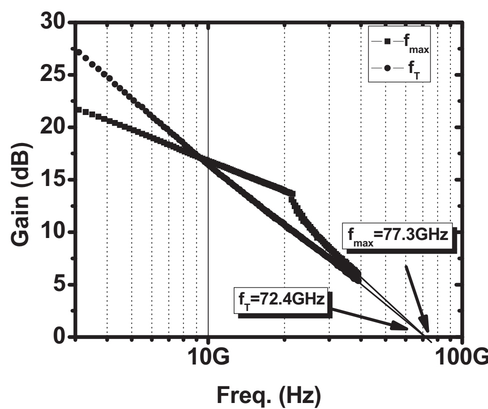

Figure.5 Current gain and MSG/MAG as a function of frequency for a 0.3×100μm^2 mHEMT.

5. Summary

In conclusion, metamorphic AlInAs/GaInAs HEMTs on silicon substrates grown by MOCVD have been fabricated successfully. In these high-quality $Ga_{0.47}In_{0.53}As$ QW structures, the thickness of the composite metamorphic buffer was less than 2μm and the buffer effectively accommodates the lattice mismatch between the HEMT devices and the silicon substrate. A depletion-mode mHEMT exhibits a saturated peak DC trans-conductance of 739mS/mm and intrinsic f_T of 72.4GHz at V_{DS}=1.0V and V_{GS}=-0.9V. Material properties and device characteristics of III-V HEMTs on Si show that this technology brings great potential for integration of high-speed III-V logic and CMOS.

Acknowledgments

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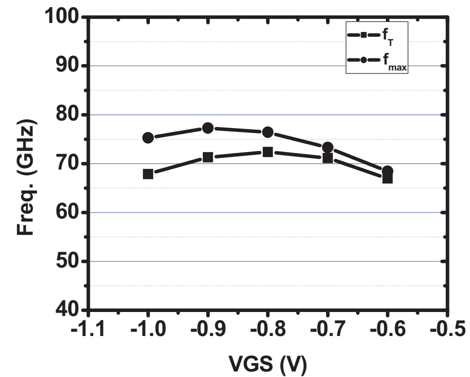

Figure.6 f_T and f_{max} at different gate-source bias voltage.

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